PERFORMANCE ANALYSIS OF SYMMETRICAL AND ASYMMETRICAL CONFIGURATION OF OPEN-END WINDING INDUCTION MOTOR DRIVE USING DECOUPLED SVPWM TECHNIQUES

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ABSTRACT

In this article, space vector based decoupled PWM techniques are proposed for both symmetrical and asymmetrical configuration of open-end winding induction motor drive. These decoupled PWM techniques are generated using instantaneous reference voltages of the two inverters. That means, one inverter reference voltages are phase shifted with respect to other inverter reference phase voltages, So that each inverter operates independently. It does not require any complex computations as in case of conventional PWM techniques. A common-mode voltage is identified in the dual inverter configuration. These decoupled PWM techniques also reduce the common mode voltage by better extent. All the proposed PWM techniques for symmetrical and asymmetrical configurations of open-end winding induction motor are implemented using MATLAB/SIMULINK and the corresponding results are reported and compared.

Keywords: *bus clamping, common-mode voltage (CMV), decoupled PWM, open-end winding induction motor drive*

1. INTRODUCTION

Pulse width modulated (PWM) inverters are widely used in past decade to control the adjustable speed drives. From the past decade different PWM techniques are proposed like sine PWM (SPWM), harmonic injection PWM and space vector PWM (SVPWM) [7]. Along with the above mentioned PWM techniques some advanced PWM techniques like bus clamping PWM and double switching bus clamping PWM techniques are also proposed in [7,8]. In case of conventional SVPWM, which is also known as center spaced PWM (CSPWM), inactive state (zero state) is used in equal intervals of time in a given sub-cycle (T_S) [5].Whereas, in case of bus clamping PWM techniques zero state is used only once in a given sub-cycle [5]-[8]. Similarly, in double switching clamping sequences instead of zero state, active state is switches twice in a sub-cycle period [8]. Pulse width modulated inverters usually produce high frequency output voltage, which causes the generation of common-mode voltage across the motor phase windings. This results the flow of bearing currents and EMI problems inside the machine [1]-[4]. To eliminate these effects different configurations are proposed from past decade given in [1]-[4]. Out of those, open-end winding induction motor is the one of the configuration, where we can directly get the three level output voltage with two conventional two level inverters on either side feeding half of the dc voltage to the each inverter compared to conventional multilevel inverters [1]. Due to this reduction in magnitude of input voltage over conventional multilevel inverters, common mode voltage is also reduced by high extent, which further reduces the bearing currents [10].

This paper presents the decoupled space vector based PWM techniques for both symmetrical and asymmetrical configurations of open-end winding induction motor drive. All the proposed PWM techniques are generated using instantaneous reference phase voltages of the inverters, i.e. INV-II phase voltages are phase shifted by 180^o with respect to INV-I phase voltages. These PWM techniques are also eliminate the common mode voltage by great extent. To validate the proposed PWM techniques several simulation studies have been carried out in MATLAB/SIMULINK and the corresponding results are presented and compared.

2. OPEN-END WINDING INDUCTION MOTOR DRIVE

To eliminate the unwanted current flow due to the common-mode voltage present in the machine open-end stator winding induction motor configuration is used [1]. Two conventional inverters are connected across on either side of open-ended induction motor drive with half of the dc voltage is applied to each inverter compared to conventional multilevel inverters. This results the voltage stress on each switch is reduced over conventional multilevel inverters [1]-[4]. The schematic of open-ended induction motor drive is shown in Fig. 1 [1].

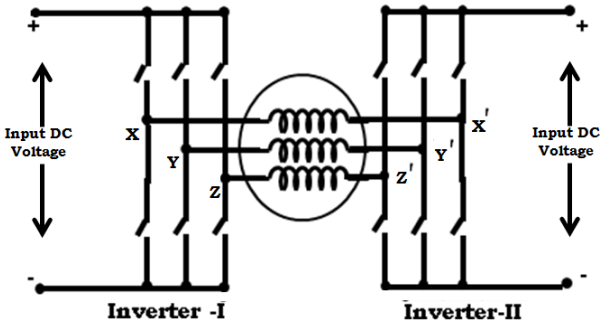

Fig. 1 Schematic of open-ended induction motor drive

In the proposed work, two configurations are proposed for open-end winding induction motor drive.

2.1. Symmetrical Configuration

In this configuration, equal amount of dc voltage (Vdc/2) is applied across the two conventional inverters fed on either side of the open-ended induction motor drive to get three level operation is shown in Fig. 2.

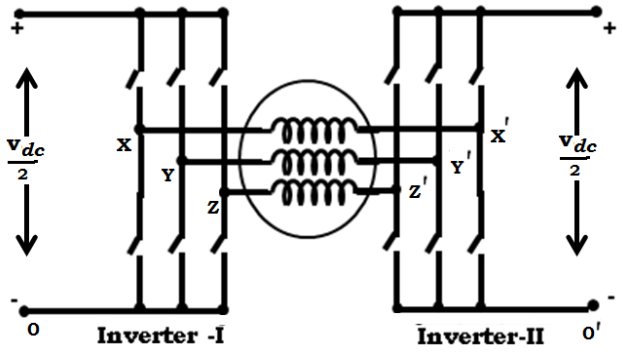

Fig. 2 Symmetrical configuration of open-ended induction motor drive

Let V_{XO},V_{YO},V_{ZO} are the pole voltages of Inv-I and $V_{X'O'}$,$V_{Y'O'}$,$V_{Z'O'}$ are the pole voltages of Inv-II respectively. The effective phase voltage is given in Eq. (1).

$$\begin{aligned} V_{XX'} &= V_{XO} - V_{X'O'} \\ V_{YY'} &= V_{YO} - V_{Y'O'} \\ V_{ZZ'} &= V_{ZO} - V_{Z'O'} \end{aligned} \tag{1}$$

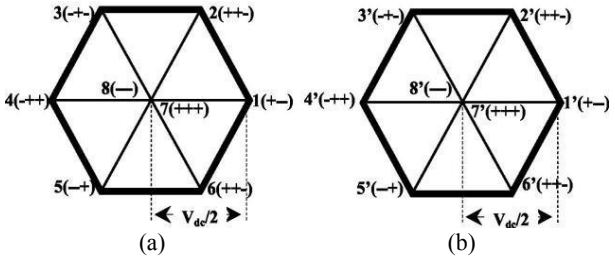

Fig. 3 Space vector locations of Inv-1 (a) and Inv-2 (b)

The sum of all the phase voltages is not equal to zero. This is due to the presence of common mode voltage in the phase windings, which leads to the flow of small amount of zero sequence ("Bearing") currents into the machine. The switching state vectors of the individual inverters are shown in Fig. 3. When switch is on represented with '+' (or) 1, when switch is off represented with '-' (or) 0. The magnitude of common mode voltage (V_{CM}) is given by

$$V_{CM} = \frac{V_{XX'} + V_{YY'} + V_{ZZ'}}{3} \tag{2}$$

2.2. Asymmetrical Configuration

In this configuration, unequal amount of dc voltage (Vdc/3 & 2Vdc/3) is applied across the two conventional inverters; so that two inverters are operates independently to get four level operation is shown in Fig. 4.

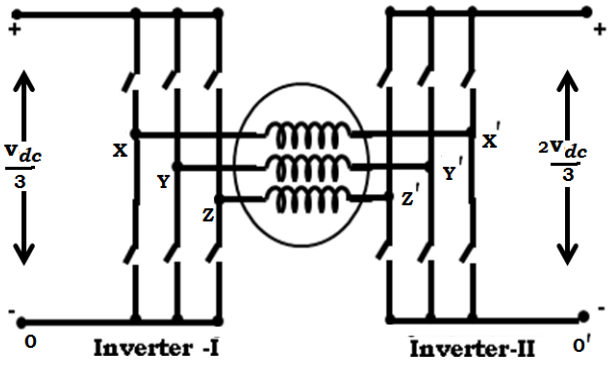

Fig. 4 Asymmetrical configuration of open-ended induction motor drive

3. DECOUPLED SVPWM TECHNIQUES

All decoupled space vector based PWM techniques proposed in this work are obtained using the instantaneous reference voltages of two inverters by phase shifting one inverter reference voltages by α^o with respect to other inverter reference voltages. In this article, decoupled bus clamping sequences are proposed along with the center spaced PWM for symmetrical and asymmetrical configurations of open-end winding induction motor drive. Decoupled bus clamping PWM sequences gives less harmonic distortion in the output voltage over center spaced PWM. Let the instantaneous reference voltages of Inv-1 and Inv-2 are given in Eq. (3) and Eq. (4) respectively.

$$\begin{aligned} V_{XREF1} &= V_m \cos(\omega t) \\ V_{YREF1} &= V_m \cos(\omega t - 120^o) \\ V_{ZREF1} &= V_m \cos(\omega t - 240^o) \end{aligned} \tag{3}$$

and

$$\begin{aligned} V_{XREF2} &= V_m \cos(\omega t + \alpha^o) \\ V_{YREF2} &= V_m \cos(\omega t - 120^o + \alpha^o) \\ V_{ZREF2} &= V_m \cos(\omega t - 240^o + \alpha^o) \end{aligned} \tag{4}$$

Where α^o is the switching angle of Inv-2 with respect to Inv-1. In the article, two switching angles (120^o & 180^o) are considered for both symmetrical and unsymmetrical configurations of open-end winding induction motor drive. In centre spaced PWM (7218), zero vector is used twice in a half carrier cycle [5-10]. To generate centre spaced sequence, Inv-1 is operated in sector-1 (0^o), whereas Inv-2 is operated by 180^o advance with Inv-1 as reference is shown in Fig. 5. Similarly, Inv-2 is operated in advance by 120^o with respect to Inv-1reference phase voltages.

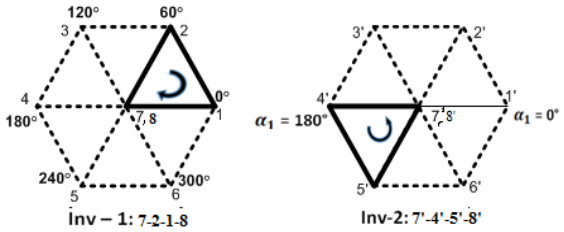

Fig. 5 Switching sequences of the individual inverters using center spaced PWM for α=180° (7218) [10]

The number of switchings per sub-cycle in center spaced PWM is equal to three [5-10]. On the other hand, in case of bus-clamping sequences(721/812) only one zero state is used in each sub-carrier cycle [6-10]. One of the phases in bus clamping techniques are clamped to either positive or negative dc rail. So the number of switchings per sub-carrier cycle is reduced to one third over center spaced PWM [6-10]. This results the reduction of switching loss by 33% and also better voltage profile across the output. Switching sequences of the two inverters using bus clamping PWM techniques for α=180° are shown in Fig. 6 and Fig. 7.

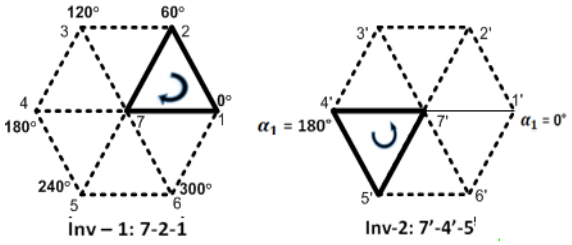

Fig. **6** Switching sequences of the individual inverters using bus clamping PWM (721) for α=180° [8]

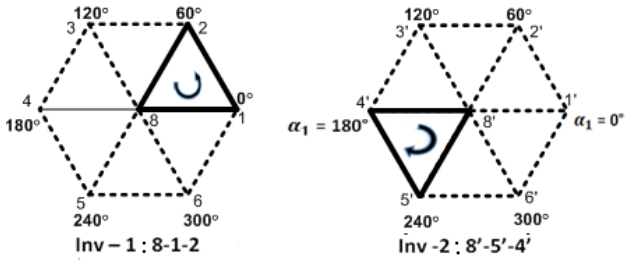

Fig. 7 Switching sequences of the individual inverters using bus clamping PWM (812) for α=180° [8]

Similarly, in double switching bus-clamping sequences only one zero state is used for sub-carrier period (T_S) But, active state is switches twice in T_S period unlike other PWM techniques [5-10]. Switching sequences for different double switching clamping sequences (7212 or 2721, 8121 or 1812,) are shown in Fig. 8 and Fig. 9.

All the proposed decoupled PWM techniques for both symmetrical and asymmetrical configurations produce considerable amount of common-mode voltage for α=180° and zero common-mode voltage for α=120° which is shown in results part.

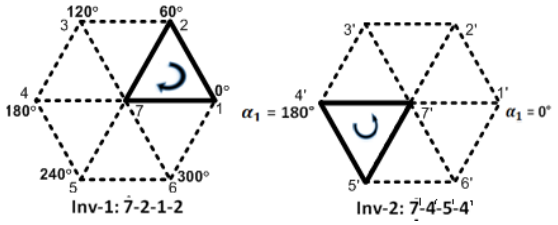

Fig. 8 Switching sequences of the individual inverters using double switching positive bus clamping PWM (7212) for α=180° [8]

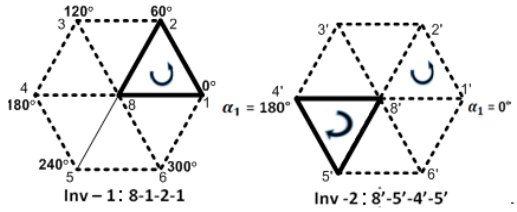

Fig. 9 Switching sequences of the individual inverters using double switching negative bus clamping PWM (8121) for α=180° [8]

4. RESULTS AND DISCUSSION

To validate the proposed decoupled space vector based PWM techniques numerous simulation studies have been carried out in MATLAB/SIMULINK. An effective DC voltage 540V is applied to the two inverters and the switching frequency is chosen as 1.5 KHz.

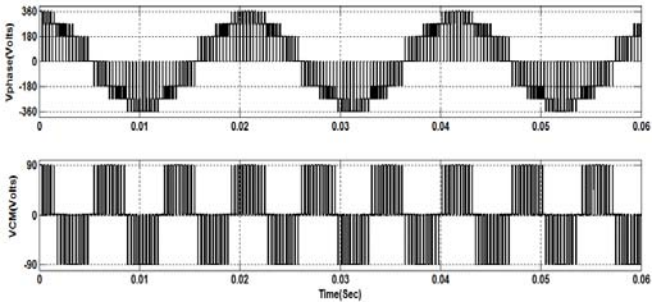

Fig. 10 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180° with center spaced PWM (Symmetrical configuration) [8]

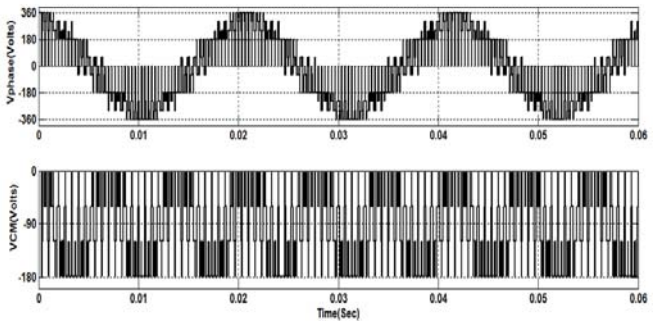

Fig. 11 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180° with center spaced PWM (Asymmetrical configuration) [8]

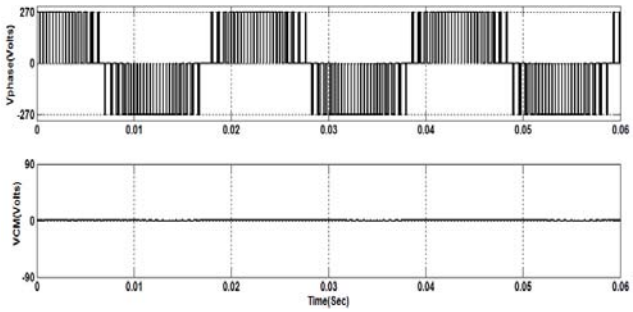

Fig. 12 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with center spaced PWM (Symmetrical configuration) [8]

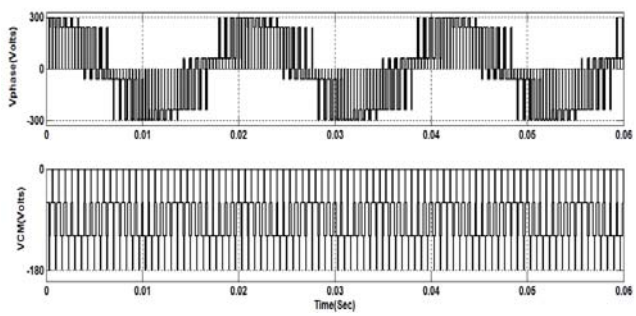

Fig. 13 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with center spaced PWM (Asymmetrical configuration) [8]

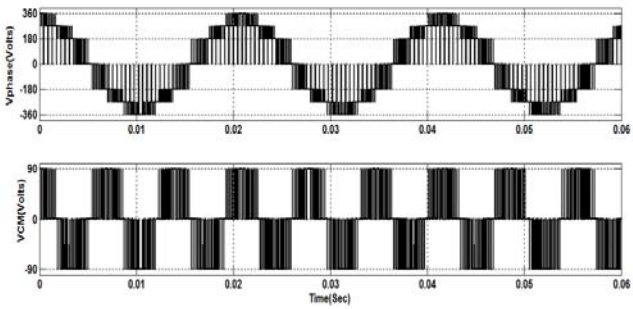

Fig. 14 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180^o with negative bus clamping PWM (812) (Symmetrical configuration) [8]

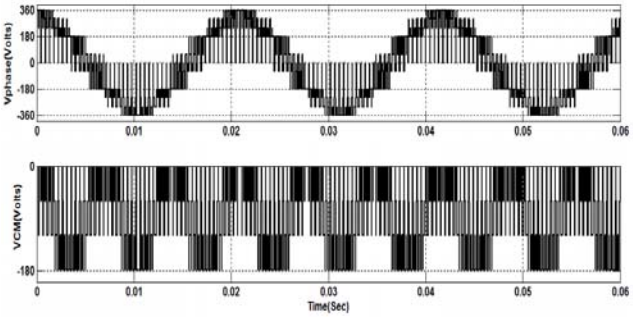

Fig. 15 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180^o with negative bus clamping PWM (812) (Asymmetrical configuration) [8]

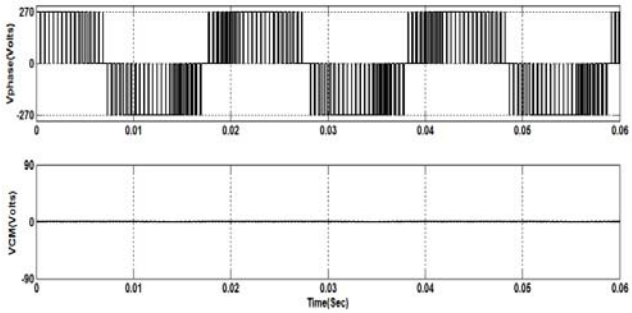

Fig. 16 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with negative bus clamping PWM (812) (Symmetrical configuration) [8]

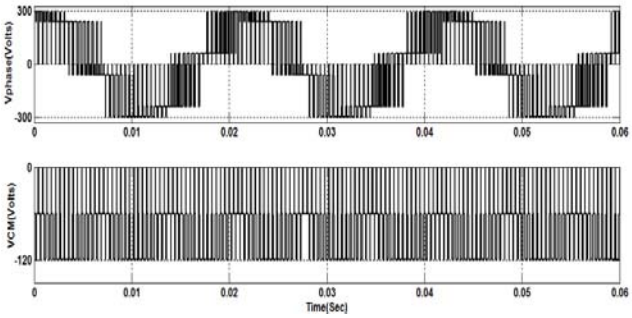

Fig. 17 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with negative bus clamping PWM (812) (Asymmetrical configuration) [8]

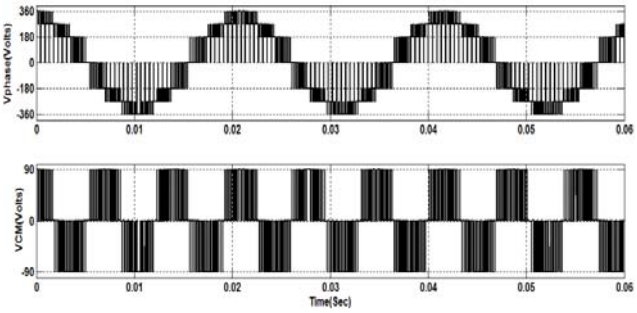

Fig. 18 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180o with positive bus clamping PWM (721) (Symmetrical configuration) [8]

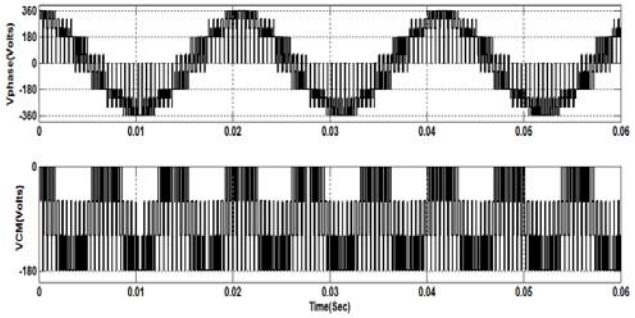

Fig. 19 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180^o with positive bus clamping PWM (812) (Asymmetrical configuration) [8]

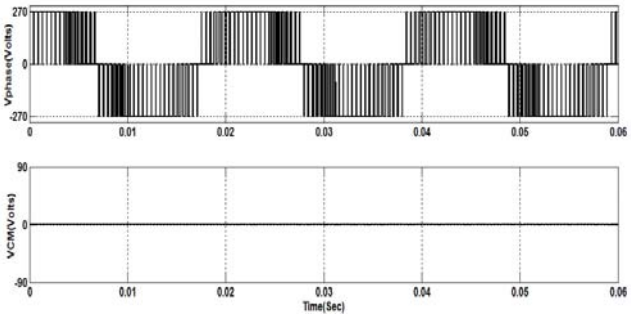

Fig. 20 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with positive bus clamping PWM (721) (Symmetrical configuration) [8]

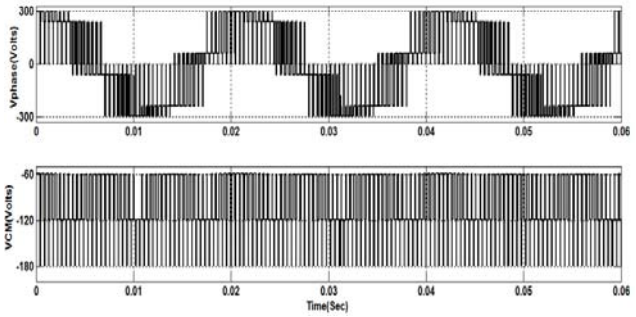

Fig. 21 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with positive bus clamping PWM (721) (Asymmetrical configuration) [8]

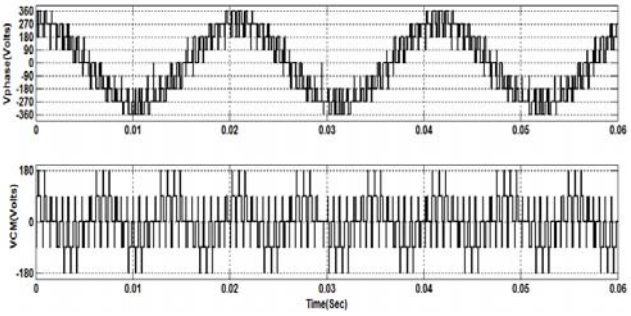

Fig. 22 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180^o with double switching negative bus clamping PWM (1812/8127) (Symmetrical configuration) [8]

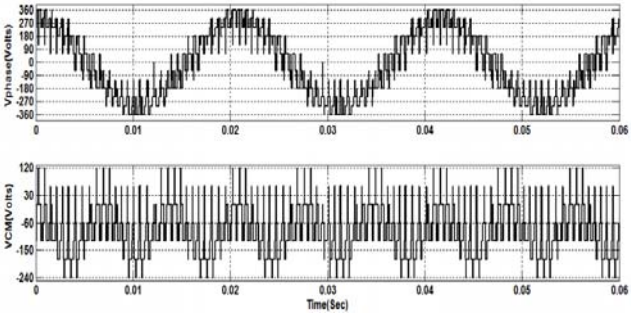

Fig. 23 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180^o with double switching negative bus clamping PWM (1812/8127) (Asymmetrical configuration) [8]

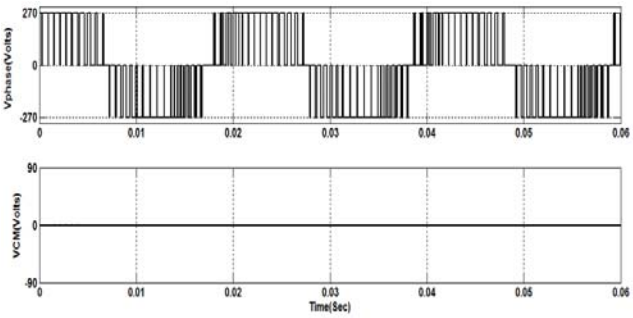

Fig. 24 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with double switching negative bus clamping PWM (1812/8127) (Symmetrical configuration) [8]

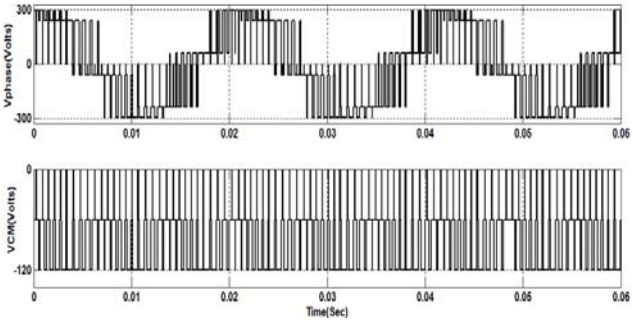

Fig. 25 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with double switching negative bus clamping PWM (1812/8127) (Asymmetrical configuration) [8]

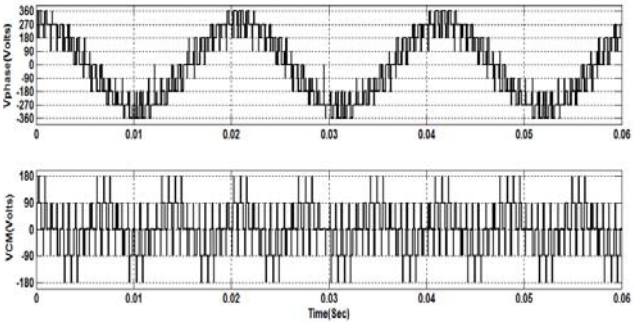

Fig. 26 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180^o with double switching positive bus clamping PWM (2721/7212) (Symmetrical configuration) [8]

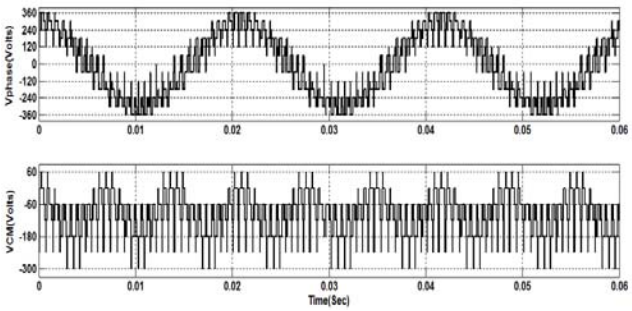

Fig. 27 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=180^o with double switching positive bus clamping PWM (2721/7212) (Asymmetrical configuration) [8]

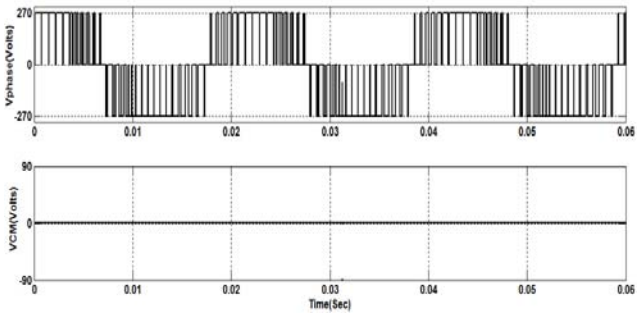

Fig. 28 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with double switching positive bus clamping PWM (2721/7212) (Symmetrical configuration) [8]

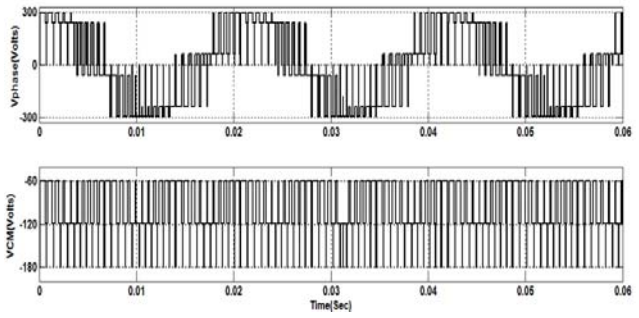

Fig. 29 Top trace (Vphase) and bottom trace common-mode voltage (VCM) for α=120^o with double switching positive bus clamping PWM (2721/7212) (Asymmetrical configuration) [8]

From Fig. 10, it can be observed that symmetrical configuration of dual Inverter fed open-end induction motor drive using center spaced PWM (8127) for α=180^o generates three level output voltage along with the common mode voltage of magnitude +Vdc/6(+90V) and -Vdc/6(-90V). Similarly in case of asymmetrical configuration, it generates four level output along with the common mode voltage of magnitude 0 and -Vdc/3(-180V) shown in Fig. 11. It is observed that the common-mode voltage is zero for all the proposed decoupled space vector PWM techniques with symmetrical configuration for α=120^o. This is because of two conventional inverters operate independently with an equal amount of dc input voltage (Vdc/2). At any instant of time both Inv-1 and Inv-2 generates an effective pole voltage of either 0 or Vdc/2. On the other hand, as in case of asymmetrical configuration the magnitude of CMV is not zero. The main reason for this is the two conventional inverters are not operated with the same input voltage (Inv-1 is 2Vdc/3and Inv-2 is Vdc/3), which leads to considerable amount of common-mode voltage is generated as per Eq. (2). It is also observed that for α=120^o common-mode voltage is absent in motor phase voltage in symmetrical configuration, which is present in asymmetrical configuration. As in case of bus clamping PWM techniques (812/721) one of the phase is clamped to either negative or positive dc rail, it results the less harmonic content in the output voltage and the corresponding CMV under this case is, +Vdc/6(+90V) and -Vdc/6(-90V) shown in Fig. 14 and Fig. 18 for symmetrical configuration. In case of asymmetrical configuration, it is –Vdc/3(-180V) and zero as shown in Fig. 15 and Fig. 19. Similarly, in double switching bus clamping sequences (1812/2721) unlike centre spaced PWM and bus clamping PWM one of the active state is switches twice in a sub-cycle period (T_S). It is observed from Fig. 22, Fig. 23, Fig. 26 and Fig. 27 that the profile of output voltage is improved in double switching bus clamping sequences over other decoupled PWM techniques proposed in this work, i.e. magnitude of step change is less over remaining PWM techniques. It results the quality of output voltage is improved. All PWM techniques proposed in this article gives zero common mode voltage for switching angle α=120^o with symmetrical configuration. In case of asymmetrical configuration, for α=120^{o}all bus clamping PWM techniques generates less common mode voltage of peak magnitude +2Vdc/9 or -2Vdc/9 (+120V or -120V) than centre spaced PWM technique (180V). Similarly, in asymmetrical configuration for α=180^o double switching clamping sequences generate high common mode voltage of peak magnitude2Vdc/3(360V) than remaining cases, but Output voltage profile is improved shown in Table 1.

Table 1 THD values of output voltage and peak to peak magnitude of CMV for different PWM techniques

Symmetrical Configuration				Asymmetrical Configuration	
Sequence / α ^{o}		V_{THD} (%)	VCM P-P (V)	V_{THD} (%)	VCM P-P (V)
8127	180 ^{o}	22.58	180	22.71	180
	120 ^{o}	23.65	0	23.63	120
812	**180 ^{o}**	**8.72**	**180**	**9.12**	**180**
	120 ^{o}	**11.74**	**0**	**11.76**	**120**
721	**180 ^{o}**	**8.73**	**180**	**9.08**	**180**
	120 ^{o}	**11.63**	**0**	**11.64**	**120**
1812	180 ^{o}	10.13	360	11.16	360
	120 ^{o}	17.39	0	17.38	120
2721	180 ^{o}	10.13	360	11.17	360
	120 ^{o}	17.37	0	17.37	120

5. CONCLUSION

In this article, space vector based decoupled PWM techniques have been implemented for symmetrical and asymmetrical configuration of open-end induction motor drive. All PWM techniques are generated by phase shifting the one inverter reference voltages by 180^o and 120^o with respect to other inverter along with the simple digital logic. Common mode voltage is identified in the open-end induction motor drive. In symmetrical configuration, for a switching angle of 120^o common mode voltage is completely nullified, which is the main aim of this work. Similarly in asymmetrical configuration, common mode voltage is not completely nullified. In symmetrical configuration both center spaced and bus clamping PWM techniques generates reduced CMV over double switching PWM techniques for a switching angle of 180^o. But, double switching bus clamping PWM techniques gives better voltage profile than other proposed PWM techniques. Whereas, bus clamping PWM techniques gives less harmonic distortion in output voltage for both symmetrical and asymmetrical configurations for a switching angle of 180^o.

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Received July 27, 2017, accepted October 22, 2017

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