VOLTAGE DOUBLER FOR AC-DC STEP-UP LINEAR POWER SUPPLIES: DESIGN, MODELLING AND SIMULATION

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ABSTRACT

This paper focuses on the design, modelling and simulation of voltage multiplier circuits for step-up AC-DC linear power supplies. The voltage multiplier is commonly used in applications that require the conversion of an AC low voltage to a very high DC voltage. Those applications require very low currents, thus, the capacitor selection is not an issue. However, when the voltage multiplier is part of a power supply, the load current becomes larger, which makes the capacitors selection more difficult. To help designers in the capacitors selection some design formulas are presented. Simultaneously, a simple simulation technique that is able to predict the circuit behaviour will be presented, revealing also essential for the design process.

Keywords: *power supplies, linear regulator, voltage multiplier and capacitors*

1. INTRODUCTION

Power supplies can be subdivided in *AC-DC* converters, *DC-DC* converters, *DC-AC* converters and *AC-AC* converters.

The majority of electronic devices are powered from a *DC* power source, so, the first two groups are the most common [1].

DC power supplies can be subdivided in linear power supplies and switched mode power supplies.

The linear power supplies are simple, durable, deliver power with low noise, have an excellent line and load regulation, a very good response time to load and line changes and low *EMI* [1, 2]. These power supplies contain a transformer, a rectifier, a filter and a regulator (Fig. 1).

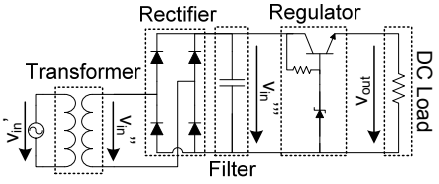

Fig. 1 *AC-DC* linear power supply

The transformer ensures electrical isolation between *AC* primary source and the output of the power supply, and, simultaneously, step-down the voltage and step-up the current [3]. The relationship between the amplitude of the input (v_{in}') and the output voltage (v_{in}'') of the transformer has standard values.

The bridge rectifier converts the incoming *AC* line voltage into a *DC* voltage, with high harmonic content. The filter smooths the ripple of the rectified voltage, reducing the output voltage ripple and simultaneously increases the output voltage mean value. Finally, the regulator converts the unregulated *DC* voltage (v_{in}''') into a regulated one (v_{out}). The regulator holds the output voltage constant independently of the line, the *DC* load and the temperatures changes.

The regulator operates has a variable resistor, thus, both regulator and the *DC* load represent a voltage divider, which means that the output voltage, v_{out}, is lower than v_{in}'''. The previous analyses allow us to conclude that v_{out} cannot exceed the amplitude of v_{in}'', so, v_{out} value is limited by the transformer turns ratio.

However, if the rectifier is replaced by a voltage multiplier, it is possible to convert the *AC* voltage (v_{in}'') into a higher *DC* voltage (v_{in}'''). Fig. 2 shows an *AC-DC* step-up linear power supply.

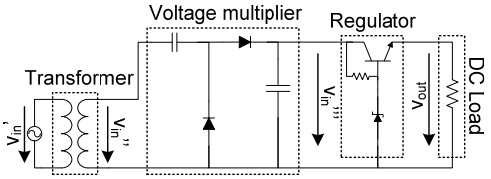

Fig. 2 *AC-DC* step-up linear power supply

The voltage multiplier converts the *AC* electrical power from a lower voltage (v_{in}'') to a higher *DC* voltage (v_{in}''') using a network of capacitors and diodes. This circuit is commonly used in high-voltage and very low current applications typically lower than 5 *mA* [4]. The voltage multiplier is commonly used in *CRT* circuits [4], in high voltage pulse applications used in many industries such as plasma, ozone making, sterilization, food processing, water treatment and military applications [5, 6] and in *HV* generators for medical *X-ray* machine [7]. In such circuits, the capacitors selection depends on the frequency of the input signal. If the voltage multiplier is used in a high frequency application (10 *kHz*), the capacitors used are in the range of 20 *nF* to 60 *nF* [4].

However, in a linear power supply, the load current is much higher than 5 *mA*, which means that the capacitors used in the voltage multiplier must be chosen appropriately. In the following sections we will address this subject.

For this purpose, in the following sections some formulas will be presented, that will prove to be very useful in the selection of the capacitors. Simultaneously, a simple simulation technique that is able to predict the

circuit behavior will be presented. This technique reveals fundamental for the computation of some key parameters for design purposes, such as [4]:

- For the capacitors: the current *rms* value and the maximum voltage.
- For each rectifier: the maximum instantaneous reverse voltage, the peak forward surge current, the maximum forward current and the maximum forward voltage.

2. VOLTAGE MULTIPLIER ANALYSIS

The voltage multiplier under analysis, a voltage doubler, is capable of producing a *DC* voltage that is equal to twice the amplitude of the *AC* input voltage (Fig. 3).

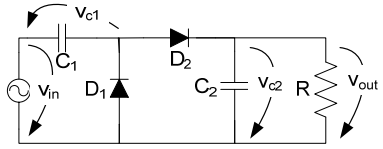

Fig. 3 Voltage doubler connected to a resistive load (*R*)

2.1. First approximation

In this section it will be applied the first approach, which uses the following assumptions:

- Capacitor C_1 will not discharge.
- Capacitor C_2 charges instantaneously.
- Capacitor C_2 will discharge linearly.

Using linear approach ($C_2 \cdot R >> 0.02$), it is possible to define capacitor C_2 voltage as, $v_{C2}(t)$:

$$v_{C2}(t) \cong v_{C2}(0) \cdot \left(1 - \frac{t}{R \cdot C_2}\right) \tag{1}$$

where: $v_{C2}(0)$ – capacitor initial voltage, R – load resistor and C_2 – capacitor capacitance.

The previous equation allows for the computation of both *ripple*, Δv_{out}, and mean value of the output voltage, $\langle v_{out} \rangle$.

$$\begin{cases} \langle v_{out} \rangle \cong v_{C2}(0) - \dfrac{\Delta v_{out}}{2} \\ \Delta v_{out} \cong v_{C2}(0) \cdot \left(\dfrac{1}{R \cdot C_2 \cdot f}\right) \end{cases} \tag{2}$$

Since capacitor C_1 will not discharge, it is possible to write:

$$v_{C2}(0) \cong 2 \cdot V_{in} - 2 \cdot V_\gamma \Rightarrow$$
$$\Rightarrow \begin{cases} \langle v_{out} \rangle \cong \left(2 \cdot V_{in} - 2 \cdot V_\gamma\right) \cdot \left(1 - \dfrac{1}{2 \cdot R \cdot C_2 \cdot f}\right) \\ \Delta v_{out} \cong \left(\dfrac{2 \cdot V_{in} - 2 \cdot V_\gamma}{R \cdot C_2 \cdot f}\right) \end{cases} \tag{3}$$

where: V_{in} – amplitude of input voltage and V_γ – diode knee voltage.

2.2. Second approximation

In this section it will be applied the second approach, which uses the following assumptions:

- Capacitor C_1 will discharge linearly.
- Capacitor C_2 will not charge instantaneously.
- Capacitor C_2 will discharge linearly.

Although capacitor C_1 discharges, at this time, it is not possible to determine the voltage loss during the discharge period. Therefore, at this time, it will be considered that capacitor C_2 initial voltage, $v_{C2}(0)$, is equal to:

$$\begin{cases} V_{C1\min} \cong V_{in} - V_\gamma \\ v_{C2}(0) \cong V_{C1\min} + V_{in} - V_\gamma \end{cases} \tag{4}$$

On the other hand, capacitor C_2 will not charge instantaneously, thus, it is necessary to compute the period of time that the capacitor requires to charge, t_{char}. For this purpose, it will be necessary to define the functions of capacitor voltage during the charging period (v_{c2char}) and during the discharging period (v_{c2disc}).

$$\begin{cases} v_{C2\,ch\arg} \cong V_{C1\min} - V_\gamma + V_{in} \cdot \cos\left(2 \cdot \pi \cdot f \cdot t - 2 \cdot \pi\right) \\ v_{C2\,disc} \cong v_{C2}(0) \cdot \left(1 - \dfrac{t}{R \cdot C_2}\right) \end{cases} \tag{5}$$

The function $v_{c2charg}$ can be simplified using the following approximation [8]:

$$\cos(x) = \sum_{k=0}^{\infty} (-1)^k \cdot \frac{x^{2 \times k}}{(2 \cdot k)!} \Rightarrow$$
$$x << 1 \Rightarrow \cos(x) \cong 1 - \frac{x^2}{2!} \Rightarrow \tag{6}$$
$$\begin{cases} v_{C2\,ch\arg} \cong V_{C1\min} - V_\gamma + V_{in} \cdot \left(1 - \dfrac{x^2}{2!}\right) \\ x = 2 \cdot \pi \cdot f \cdot t - 2 \cdot \pi \end{cases}$$

Therefore, by matching $v_{c2charg}$ and v_{c2disc}, it is possible to compute the capacitor discharge period, t_{disc}, as follows:

$$\begin{cases} K_1 = 2 \cdot \pi^2 \cdot f^2 \cdot V_{in} \\ K_2 = -\dfrac{V_{C1\min} + V_{in} - V_\gamma}{R \cdot C_2} - 4 \cdot \pi^2 \cdot f \cdot V_{in} \\ K_3 = 2 \cdot \pi^2 \cdot V_{in} \end{cases}$$
$$t_{disc} \cong \frac{-K_2 - \sqrt{K_2^2 - 4 \cdot K_1 \cdot K_3}}{2 \cdot K_1} \tag{7}$$

The time-period that C_2 takes to charge, t_{char}, is equal to:

$$t_{char} \cong \frac{1}{f} - t_{disc} \tag{8}$$

In this way, using a linear approach, it is possible to compute the output voltage *ripple* as:

$$\Delta v_{out} \cong \frac{v_{C2}(0)\cdot t_{disc}}{R\cdot C_2} \tag{9}$$

To compute the mean value of the output voltage it is necessary to know the voltage loss in C_1 during the discharging period. For that, it is necessary to compute the capacitor C_1 current during the discharging period, i_{C1disc}.

$$\begin{aligned} i_{C1disc} &\cong \frac{\langle v_{C2charg}\rangle}{R} + i_{C2charg} \\ i_{C1disc} &\cong \frac{v_{C2}(0) - \frac{\Delta v_{out}}{2}}{R} + C_2\cdot\frac{\Delta v_{out}}{t_{char}} \Rightarrow \\ i_{C1disc} &\cong \frac{\left(V_{C1min} + V_{in} - V_\gamma\right) - \frac{\Delta v_{out}}{2}}{R} + C_2\cdot\frac{\Delta v_{out}}{f^{-1} - t_{disc}} \end{aligned} \tag{10}$$

where: V_{C1min} – the minimum value of capacitor C_1 voltage during steady-state regime, $\langle v_{C2charg}\rangle$ – the mean value of capacitor C_2 voltage during the charging period in steady-state regime and $i_{C2charg}$ – capacitor C_2 current during the charging period in steady-state regime.

It is important to notice that capacitor C_1 discharges when capacitor C_2 charges. Thus, it is possible to compute capacitor C_1 *ripple* voltage as, Δv_{c1}:

$$\Delta v_{C1} \cong \frac{i_{C1disc}\cdot\left(f^{-1} - t_{disc}\right)}{C_1} \tag{11}$$

The previous value represents the voltage loss in C_1 during the discharging period. Thus, it is possible to compute the output mean value, $\langle v_{out}\rangle$, as well as the new value of V_{c1min}:

$$\begin{aligned} V_{C1min} &= V_{in} - V_\gamma - \Delta v_{C1} \\ v_{C2}(0) &= V_{C1min} + V_{in} - V_\gamma = 2\cdot V_{in} - 2\cdot V_\gamma - \Delta v_{C1} \\ \langle v_{out}\rangle &\cong v_{C2}(0)\cdot\left(1 - \frac{t_{disc}}{2\cdot R\cdot C_2}\right) \end{aligned} \tag{12}$$

At this point, it is possible to compute the output voltage ripple more accurately.

$$\Delta v_{out} \cong \frac{v_{C2}(0)\cdot t_{disc}}{R\cdot C_2} \tag{13}$$

3. VOLTAGE DOUBLER DESIGN

Section 2.2 allows us to obtain a set of formulas that can be used in the design of a voltage doubler.

In the design of this circuit two basic specifications will be considered: the average value of the output voltage, $\langle v_{out}\rangle$, and its voltage ripple, Δv_{out}.

Initially, the value of the capacity of C_2 will be computed, because this value will affect the selection of capacitor C_1, and for that equation (3) can be used.

$$C_2 \geq \left(\frac{2\cdot V_{in} - 2\cdot V_\gamma}{R\cdot\Delta v_{out}\cdot f}\right) \tag{14}$$

The above formula is oversized, since, $v_{C2}(0)$ is greater than a real one and the discharging period is maximum.

Afterwards, it will be possible to compute C_1 minimum value using equations (10) and (11).

$$\begin{cases} t_{disc} \cong \dfrac{-K_2 - \sqrt{K_2^{\,2} - 4\cdot K_1\cdot K_3}}{2\cdot K_1} \rightarrow \text{see (7)} \\ \Delta v_{out} \geq \left(\dfrac{2\cdot V_{in} - 2\cdot V_\gamma}{R\cdot C_2\cdot f}\right) \\ \Delta v_{C1} = 2\cdot V_{in} - 2\cdot V_\gamma - \langle v_{out}\rangle - \dfrac{\Delta v_{out}}{2} \\ i_{C1disc} \cong \dfrac{v_{C2}(0) - \frac{\Delta v_{out}}{2}}{R} + C_2\cdot\dfrac{\Delta v_{out}}{f^{-1} - t_{disc}} \\ \boxed{C_1 \geq \dfrac{i_{C1disc}\cdot\left(f^{-1} - t_{disc}\right)}{\Delta v_{C1}}} \end{cases} \tag{15}$$

The capacitances obtained from the previous formulas should be oversized. Afterwards, it will be presented an algorithm that improves the selection of capacitors capacitance.

3.1. Algorithm for more accurate design

The following algorithm allows for the selection of smaller capacitance capacitors and simultaneously respecting the original specifications.

In order to understand the algorithm it is important to provide some definitions.

- MAX_ERROR_ripple – is the largest permissible difference between the computed value and the specified output voltage ripple.
- MAX_ERROR_mean – is the largest permissible difference between the computed value and the specified mean value of the output voltage.
- CALC_ripple – is the computed value of the output voltage ripple.
- SPEC_ripple – is the specified value of the output voltage ripple.
- CALC_mean – is the computed mean value of the output voltage.
- SPEC_mean – is the specified mean value of the output voltage.
- ERROR_ripple = CALC_ripple - SPEC_ripple.
- ERROR_mean = CALC_mean - SPEC_mean.
- INC_C1 – increment/decrement of C_1 capacitance.
- INC_C2 – increment/decrement of C_2 capacitance.
- I_{C1desc} – capacitor C_1 current during C_1 discharge period.

Before using the previous algorithm it is necessary to compute the first iteration, which provides the initial capacitance of both capacitors (C_{10} and C_{20}), and for that, equations (14) and (15) should be used. Using the previous values together with (11) it is possible to compute capacitor C_1 voltage ripple (ΔV_{C1}).

Afterwards, the algorithm will be presented.

$$INC\_C1 = 10^{-6}$$
$$INC\_C2 = 2 \cdot 10^{-6}$$
$$SPEC\_ripple = 1.6;$$
$$SPEC\_mean = 38;$$
$$MAX\_ERROR\_ripple = SPEC\_ripple / 1000$$
$$MAX\_ERROR\_mean = SPEC\_mean / 1000$$
$$ERROR\_ripple = 2 \cdot MAX\_ERROR\_ripple$$
$$ERROR\_mean = 2 \cdot MAX\_ERROR\_mean$$
$$while \begin{pmatrix} |ERROR\_ripple| \geq MAX\_ERROR\_ripple \\ and \\ |ERROR\_mean| \geq MAX\_ERROR\_mean \end{pmatrix}$$
$$V_{C20} = 2 \cdot V_{in} - 2 \cdot V_{\gamma} - \Delta V_{C1}$$
$$K_1 = 2 \cdot \pi^2 \cdot f^2 \cdot V_{in}$$
$$K_2 = -\frac{V_{C20}}{R \cdot C_2} - 4 \cdot \pi^2 \cdot f \cdot V_{in}$$
$$K_3 = 2 \cdot \pi^2 \cdot V_{in}$$
$$t_x = \frac{-K_2 - \sqrt{K_2^2 - 4 \cdot K_1 \cdot K_3}}{2 \cdot K_1}$$
$$CALC\_ripple = \frac{V_{C20} \cdot t_x}{R \cdot C_2}$$
$$i_{C1desc} = \frac{C_2 \cdot CALC\_ripple}{f^{-1} - t_x} + \frac{V_{C20} - \frac{CALC\_ripple}{2}}{R}$$
$$\Delta V_{C1} = \frac{i_{C1desc} \cdot \left(f^{-1} - t_x \right)}{C_1}$$
$$CALC\_mean = 2 \cdot V_{in} - 2 \cdot V_{\gamma} - \Delta V_{C1} - \frac{CALC\_ripple}{2}$$
$$ERRO\_ripple = CALC\_ripple - SPEC\_ripple$$
$$ERRO\_mean = CALC\_mean - SPEC\_mean$$
$$if \left(ERRO\_ripple > 0 \right)$$
$$C_2 = C_2 + INC\_C2$$
$$else$$
$$C_2 = C_2 - INC\_C2$$
$$end$$
$$if \left(ERRO\_mean > 0 \right)$$
$$C_1 = C_1 - INC\_C1$$
$$else$$
$$C_1 = C_1 + INC\_C1$$
$$end$$
$$end$$

4. VOLTAGE DOUBLER SIMULATION

In this section a simple simulation technique will be presented, which has the following steps:

1. Draw the whole circuit and its components.
2. Identify all the states.
3. Recognize the conditions that satisfy the occurrence of each state.
4. Analyze each state, and get the mathematical equations that describe its operation.
5. Represent the sequence of states in the form of an algorithm.

Fig. 3 shows the circuit under analysis (voltage doubler), which has three different states:

- State 1 – Diode D_1 conducts and Diode D_2 do not conduct.
- State 2 – Diode D_2 conducts and Diode D_1 do not conduct.
- State 3 – None of the diodes conducts.

Afterwards, the conditions that determine the occurrence of each state, are presented:

- The first state occurs when:
  $v_{in} + v_{C1} \leq -V_{\gamma}$ and $v_{in} + v_{C1} - v_{C2} < V_{\gamma}$
- The second state occurs when:
  $v_{in} + v_{C1} > -V_{\gamma}$ and $v_{in} + v_{C1} - v_{C2} \geq V_{\gamma}$
- The third state occurs when:
  $v_{in} + v_{C1} > -V_{\gamma}$ and $v_{in} + v_{C1} - v_{C2} < V_{\gamma}$

Subsequently, each state will be analyzed.

4.1. State Analysis

Fig. 4 shows the equivalent circuit corresponding to the first state.

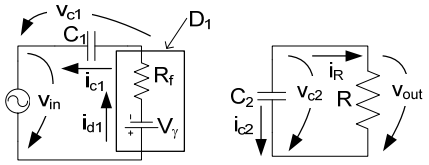

Fig. 4 Equivalent circuit corresponding to the first state

It is convenient to represent the diode (D_1) by its large-signal model, (diode model when *forward bias* – [R_f + V_γ]), in order to evaluate the currents and voltages in the network using standard analysis methods [9].

From the analysis of the previous circuit it is possible to write the resulting equations:

$$\begin{cases} v_{in} + v_{c1} + V_{\gamma} + R_f \cdot i_d = 0 \\ i_d = i_{c1} = C_1 \cdot \dfrac{dv_{c1}}{dt} \\ i_{c2} = -i_R = -\dfrac{v_{c2}}{R} = C_2 \cdot \dfrac{dv_{c2}}{dt} \end{cases} \quad (16)$$

Fig. 5 shows the equivalent circuit corresponding to the second state.

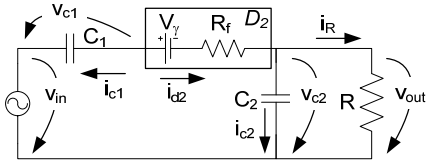

Fig. 5 Equivalent circuit corresponding to the second state

From the analysis of the previous circuit it is possible to write the following equations:

$$\begin{cases} v_{in} - v_{c1} + V_{\gamma} + R_f \cdot (-i_{c1}) + v_{c2} = 0 \\ i_{c1} = -i_{c2} - \dfrac{v_{c2}}{R} \\ i_{c2} = C_2 \cdot \dfrac{dv_{c2}}{dt} \\ i_{c1} = C_1 \cdot \dfrac{dv_{c1}}{dt} \end{cases} \quad (17)$$

Fig. 6 shows the equivalent circuit corresponding to the third state.

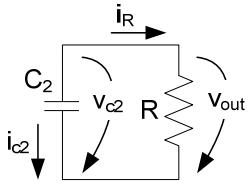

Fig. 6 Equivalent circuit corresponding to the third state

From the analysis of the previous circuit it is possible to write the following equation:

$$i_{c2} = -i_R = -\frac{v_{c2}}{R} = C_2 \cdot \frac{dv_{c2}}{dt} \quad (18)$$

4.2. Algorithm

Finally, representing the above equations, (16)-(18), in their discrete form, it is possible to develop a simulation program, which can be easily implemented in an open-source platform for numerical computation.

Following, a small algorithm is presented:

i=1

while $(i < NTP)$

if $\left(\left(v_{in}(i) + v_{c1}(i) \le -V_{\gamma} \right) \text{ and } \left(v_{in}(i) + v_{c1}(i) - v_{c2}(i) < V_{\gamma} \right) \right)$

$K_1 = R_f \cdot C_1 \quad ; \quad K_2 = R \cdot C_2$

$$v_{c1}(i+1) = -\frac{PA}{K_1} \cdot \left(v_{in}(i) + V_{\gamma} \right) + \left(1 - \frac{PA}{K_1} \right) \cdot v_{c1}(i)$$

$$v_{c2}(i+1) = \left(1 - \frac{PA}{K_2} \right) \cdot v_{c2}(i)$$

$$i_{c1}(i+1) = C_1 \cdot \frac{v_{c1}(i+1) - v_{c1}(i)}{PA}$$

$$i_{c2}(i+1) = C_2 \cdot \frac{v_{c2}(i+1) - v_{c2}(i)}{PA}$$

elseif $\left(\left(v_{in}(i) + v_{c1}(i) > -V_{\gamma} \right) \text{ and } \left(v_{in}(i) + v_{c1}(i) - v_{c2}(i) \ge V_{\gamma} \right) \right)$

$$K_3 = R_d \cdot C_2 \quad ; \quad K_4 = \frac{R_{d2}}{R} + 1 \quad ; \quad K_5 = 1 - \frac{K_4 \cdot PA}{K_3}$$

$$v_{c2}(i+1) = \frac{PA}{K_3} \cdot \left(v_{in}(i) + v_{c1}(i) - V_{\gamma} \right) + K_5 \cdot v_{c2}(i)$$

$$v_{c1}(i+1) = -\frac{PA}{C_1} \cdot i_{c2}(i) - \frac{PA}{C_1 \times R} \cdot v_{c2}(i) + v_{c1}(i)$$

$$i_{c1}(i+1) = C_1 \cdot \frac{v_{c1}(i+1) - v_{c1}(i)}{PA}$$

$$i_{c2}(i+1) = C_2 \cdot \frac{v_{c2}(i+1) - v_{c2}(i)}{PA}$$

else

$K_2 = R \cdot C_2$

$$v_{c2}(i+1) = \left(1 - \frac{PA}{K_2} \right) \cdot v_{c2}(i)$$

$$i_{c2}(i+1) = C_1 \cdot \frac{v_{c2}(i+1) - v_{c2}(i)}{PA}$$

$i_{c1}(i+1) = 0$

$v_{c1}(i+1) = v_{c1}(i)$

end

end

where:

- PA – represents the sampling period,
- NTP – represents total number of iterations (which is defined by the user).

4.3. Simulated results

In order to validate the previous analysis, as well as the simulation technique, the circuit under analysis was designed in *Matlab* using *SimPowerSytems toolbox.*

Table 1 shows the prototype characteristics.

Table 1 Characteristics of the Prototype

Components	Electrical model
Diodes (forward biased)	R_f = 0.15 Ω, V_γ = 0.86 V
C_1	C = 1902 μF
C_2	C = 4588 μF
Primary Source	Vin = 22 V (amplitude)
DC Load (R_{Load})	R = 100 Ω

Both simulation results are consistent, showing that the proposed simulation technique can be used to predict the behaviour of the voltage doubler.

5. TESTING DESIGN FORMULAS AND ALGORITHM

In this section it will be assessed the applicability of the formulas and the algorithm presented in section 3. For this purpose it will be considered 4 different situations (Table 2).

Table 2 Different situations considered for assessing the applicability of the design formulas

Test	Primary source	Load
1	V_{in} = 22 *V* (amplitude) f = 50 *Hz* (frequency)	R = 1000 Ω
2		R = 500 Ω
3		R = 250 Ω
4		R = 100 Ω

In the design of the voltage doubler it will be considered two fundamental specifications:

- The average value of the output voltage: $\langle v_{out} \rangle$ = *38 V*
- The maximum output voltage ripple: $\Delta v_{out} < 1.6$ *V*

In the following calculus, it will be considered a diode knee voltage of 0.8 *V*.

As mentioned in section 3 the design formulas (14) and (15) allow us to compute both capacitors capacitance. However, those values are oversized, and for that it was proposed the algorithm shown in section 3.1. Table 3 shows the computed values of C_1 and C_2 using the previous formulas (14-15) and the algorithm (section 3.1).

Table 3 Voltage doubler design (computed values of C_1 and C_2)

Test	Formulas		Algorithm	
	(15)	(14)		
	C_1	C_2	C_1	C_2
1	249 µF	530 µF	215 µF	462 µF
2	498 µF	1060 µF	432 µF	928 µF
3	997 µF	2120 µF	866 µF	1858 µF
4	2491 µF	5300 µF	2166 µF	4650 µF

From the analysis of the above table it is possible to conclude that the proposed algorithm (section 3.1) suggests the choice of smaller capacitors:

- Test 1 – it could be chosen the following standard capacitances: C_1 = 220 μF and C_2 = 470 μF.
- Test 2 – it could be chosen the following standard capacitances: C_1 = 470 μF and C_2 = 1000 μF.
- Test 3 – it could be chosen the following standard capacitances: C_1 = 1000 μF and C_2 = 2200 μF.
- Test 4 – it could be chosen the following standard capacitances: C_1 = 2200 μF and C_2 = 4700 μF.

Considering the standard capacitance values [10], it is possible to conclude that in the test 1, 2 and 4 the proposed algorithm suggests the choice of smaller capacitors.

The following table shows that the capacitance values computed in Table 3 satisfy the original specifications.

Table 4 Output voltage ripple and mean value computed using the proposed simulation technique

Test	Formulas		Algorithm	
	$\langle v_{out} \rangle$	Δv_{out}	$\langle v_{out} \rangle$	Δv_{out}
1	38.6 V	1.3 V	38.1 V	1.5 V
2	38.6 V	1.3 V	38.1 V	1.5 V
3	38.6 V	1.3 V	38.1 V	1.5 V
4	38.3 V	1.3 V	38.1 V	1.5 V

6. EXPERIMENTAL RESULTS

To demonstrate the applicability of the design formulas and the proposed algorithm, an experimental prototype will be considered, with the following specifications: ($\langle v_{out} \rangle$ = *38 V*, $\Delta v_{out} < 1.6$ *V*, R = 100 Ω and V_{in} = 22 V). The above specifications correspond to test 4, thus, the chosen capacitors are: C_1 = 2200 μF and C_2 = 4700 μF.

The computed capacitance values require the use of electrolytic capacitors, which typically have a tolerance of 20% [10]. It is therefore necessary to determine the electrical characteristics of the different components.

6.1. Electrical characteristics of the components

Fig. 7 show the *I-V* characteristic of the rectifiers (when forward biased).

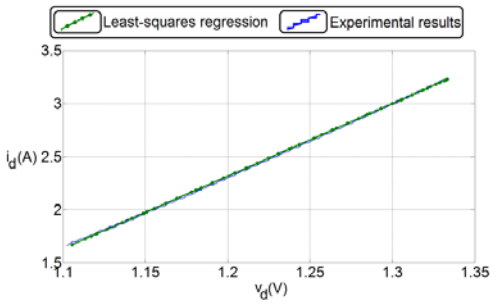

Fig. 7 Characteristic of the rectifier

Fig. 8 shows the characteristic of C_1.

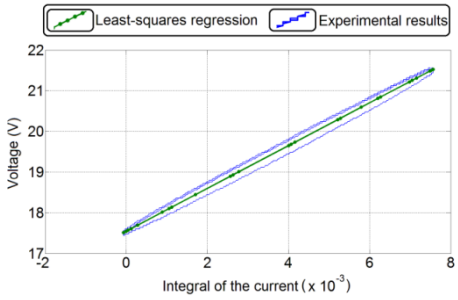

Fig. 8 Characteristic of capacitor C_1

Fig. 9 shows the characteristic of C_2.

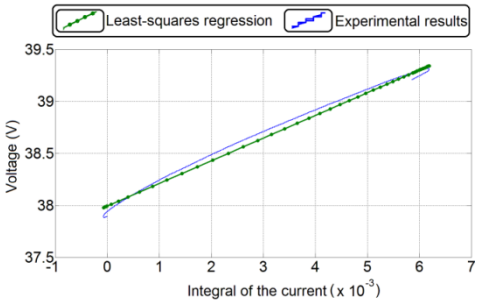

Fig. 9 Characteristic of capacitor C_2

Using least-squares regression it is possible to compute the characteristic of the rectifiers and capacitors (Table 1).

6.2. Comparison between experimental and simulated results

It should be also mentioned that the input voltage waveform of the voltage doubler is not exactly sinusoidal (Fig. 10a). Thus, for validation purpose, it was used an

waveform approximately equal to the real input voltage (Fig. 10b).

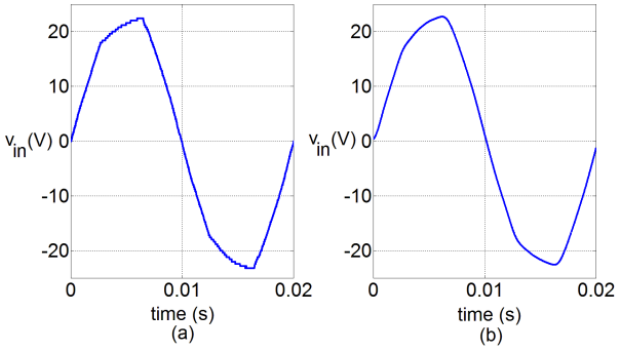

Fig. 10 Voltage waveform at the secondary of the transformer (v_{in}): (a) experimental waveform and (b) filtered experimental waveform

The experimental waveform of v_{in} has some noise, hence, it was necessary to smooth it, and for that, it was used a low pass filter (Fig. 10b).

Finally, considering the previous waveform, together with the characteristics of the components obtained experimentally, it is possible to compare the experimental results with the simulated ones.

Fig. 11, 12, 13, 14, 15 and 16 show both experimental and simulated waveforms of capacitor C_1 voltage, of capacitor C_1 current, of diode D_1 current, of diode D_2 current, of capacitor C_2 voltage and of capacitor C_2 current, respectively, during steady state regime.

The following curves are essential in the design process:

- For the capacitors: the simulated waveform of capacitor current and voltage enable the computation of current *rms* value and the maximum voltage.

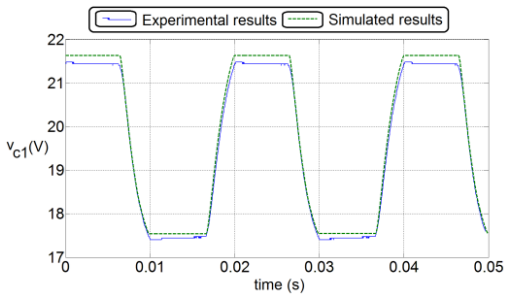

Fig. 11 Capacitor C_1 voltage waveform (v_{c1})

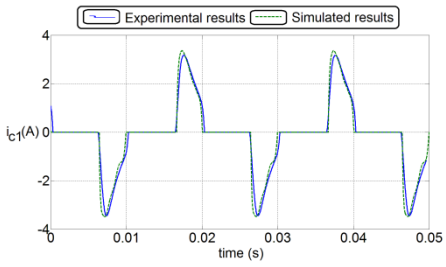

Fig. 12 Capacitor C_1 current waveform (v_{c1})

- For each rectifier: the simulated waveform of diodes current and voltage enables the computation of the maximum instantaneous reverse voltage, the peak forward surge current, the maximum forward current and the maximum forward voltage.

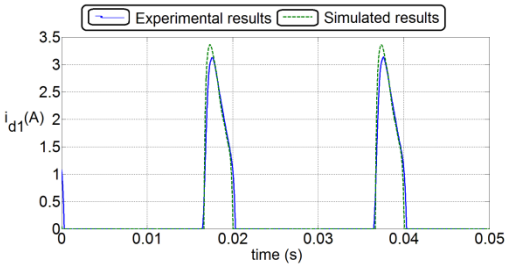

Fig. 13 Diode D_1 current waveform (i_{d1})

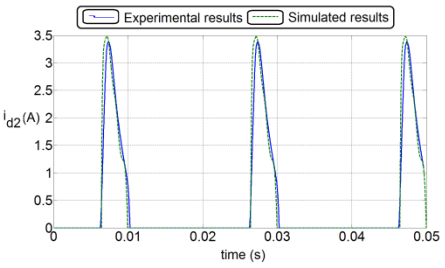

Fig. 14 Diode D_2 current waveform (i_{d2})

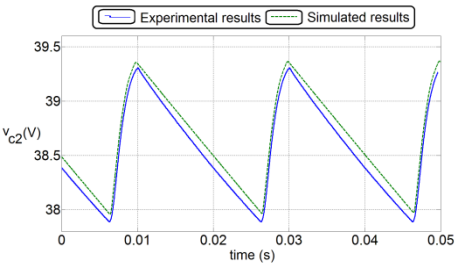

Fig. 15 Capacitor C_2 voltage waveform (v_{c2})

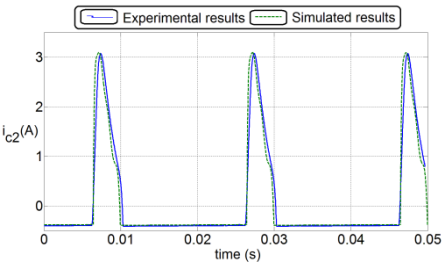

Fig. 16 Capacitor C_2 current waveform (i_{c2})

Both simulated and experimental waveforms agree, as expected.

6.3. Results analysis

The choice of the capacitors used in the experimental prototype had in consideration the proposed algorithm (Table 3), and the initial specifications ($\langle v_{out} \rangle$ = 38 *V* and Δv_{out}= 1.6 V).

Fig. 15 shows that the ripple specification ($\Delta v_{out} < 1.6$ *V*) was fulfilled; the ripple of the experimental prototype was equal to 1.42 *V*.

However, the average voltage is slightly higher than the specified one ($\langle v_{out} \rangle = 38$ *V*). The average voltage of the experimental prototype was equal to 38.6 *V*. This difference is due to the fact that the *r.m.s.* of the input voltage (Fig. 10) is higher than the *r.m.s.* of a pure sine wave.

7. CONCLUSIONS

This article discusses the design of voltage doublers for step up linear power supplies. The voltage doubler is commonly used in applications that require low currents. In such cases the capacitor selection is not an issue.

However, linear power supplies demand high current values, which make the capacitors selection complex.

In this paper some design formulas were presented that can be used in the capacitors selection. These formulas allow for the selection of oversized capacitors. To improve the price/performance ratio an algorithm that allows the selection of smaller capacitors was presented.

Furthermore, it was also presented a simple simulation technique that predicts the current and voltage waveforms in all components. The previous waveforms are essential for designing purposes.

The simulation technique, the design formulas and the algorithm were validated through experimental results.

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