DIGITAL PULSE GENERATOR FOR MULTIPHASE BOST CONVERTER

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ABSTRACT

The paper deals with a new method of design of digital pulse generator, which is specially designed for multiphase converters. The advantage of this control method lies in its applicability to the microcontrollers. The generator is capable of generating the PWM pulses for a variable number of legs in the range of 1-10. In the article, the results from 6 legs connection are presented. By the utilization of the several legs, the generator can generate pulses with phase shift and frequency of 50 kHz. The size of the phase shift depends on the number of legs. The paper describes the functions of the individual parts of the generator, which are shown schematically. The simulations and experimental models were built and measured to verify the theoretical assumptions. The paper contains also the PCB design and practical construction notes.

Keywords: *digital pulse generator, multiphase converters, PWM pulses*

1. INTRODUCTION

In present times, the electricity production by solar panels utilization is a very actual and discussed problem. There is a significant endeavor to improve the efficiency of energy conversion. In order to succeed, it is imperative to use a converter, which would be able to obtain the maximum energy from the solar panel. Such type of a converter is represented by the connection of multiphase converter, described in [1], [2]. For its control, a pulse generator, that generates pulses with individual phase shift for each leg is needed.

This paper presents a new type of digital multiphase pulse generator (*DMPG*). The advantage of the proposed generator lies in its relatively simple design, high precision, low cost, wide variety of signal generation and control simplicity itself. The generator is able to generate *PWM* (**P**ulse **W**idth **M**odulation) signal with the desired frequency. In this case, it has frequency of 50 kHz. For the purpose of main DMPG properties description, the paper is divided into several chapters.

2. GENERATOR´S OPERATION PRINCIPLE

The *DMPG* consists of two basic parts. The first part is created from adjustable pulse generator and the pulse divider. The second part is constructed by the legs themselves. This part of the generator is creating the *PWM* signals.

A Pulse generator and divider

The main task of this part is to generate phase shifted signals for the proposed legs. Thus, the size of the pulse phase shift depends on the number of legs. It is important to note, that the frequency remains unchanged. The pulse generator and divider consist in total from 4-bit *BCD* (**B**inary **C**oded **D**ecimal) counter, 10-bit decoder, adjustable pulse generator and logic gates (see Fig. 1).

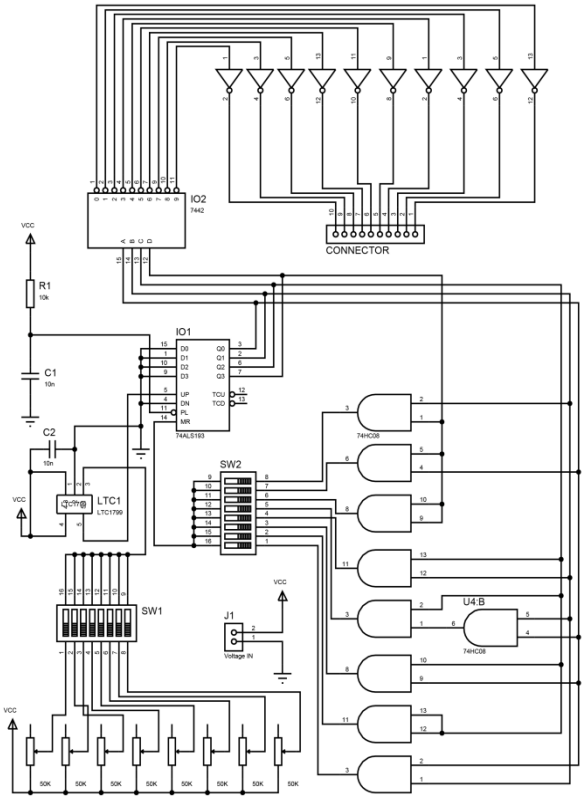

Fig. 1 Pulse generator and divider schematics

Phase shifted pulses generation is provided by two integrated circuits: 4-bit *BCD* counters IC (integrated circuit) 74193 and 10-bit decoder IC 7442. The counter is able to count from 0 to 15 in binary form. For 6 legs converter, the range of the used counter must be reduced. For the counting reduction, the logical gates of AND type with two inputs (IC 7408) are used. Into its first input, the output of the second bit of counter is connected. Into its second input, the output of the third bit of counter is connected. Thus, the counter is cleared at the moment, when combination 0110 occurs on its output bits. With such

connection, the counting range can be reduced, in dependence on the number of legs. Each change of the number of legs requires also the change of the input frequency. This requirement is fulfilled by the usage of the pulse generator based on IC type LTC1799. The frequency change in this case is reached by the change of resistor R value (see Fig.2) [3]. It is secured by the 8-bit switches array SW1 (see Fig. 1), but the important note is, that only the one switch can be in switch-on position. The rest could be only in switch-off position. This array is interconnected with the scale of potentiometers, which have set the different individual values. It is possible to calculate their rate by the following equation:

$$f_{osc} = 10 \,.\, 10^6 \cdot \left(\frac{10.10^3}{N \cdot R}\right) \quad [\text{Hz}] \tag{1}$$

For 6 legs converter and required frequency 50 kHz per one leg (300 kHz total frequency of the pulse generator), we can choose:

$$R = 10.10^6 \left(\frac{10.10^3}{N \cdot 300.10^3}\right) \tag{2}$$

where " f_{osc} " is a frequency of the pulse generator. "*R*" is the calculated resistor value for the desired frequency. The parameter "*N*" is a pulse generator constant. This constant may have values 1, 10, 100. This value depends on the connection of pulse generator *DIV* (**DIV**ider) pin, (see Fig. 2). In described case, the value of *N* is set to 100. According the equation (1), the resistance for the remaining legs is calculated, too.

$$R = 3.33\ k\Omega \tag{3}$$

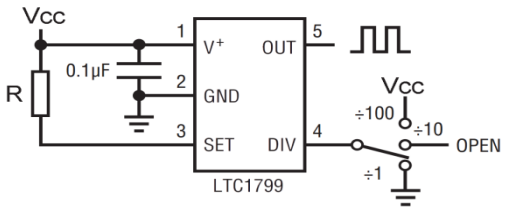

Fig. 2 Basic connection of LTC1799 pulse generator

For the different number of legs, the different clock frequency is needed, as well as different value of resistances (see Table 1).

Table 1 Frequencies and resistances for the selected number of legs

Legs num.	Frequency [kHz]	Resistance *R* [kΩ]
1	50	20
2	100	10
3	150	6.667
4	200	5
5	250	4
6	300	3.33
7	350	2.86
8	400	2.5
9	450	2.22
10	500	2

The basic frequency for one leg converter can be chosen arbitrarily, but the multi-legs connections would respect the multiply effect of basic frequency given by Table 1.

If the number of legs is changed, the counting range of IC 74193 counter has to be changed, too. This change is provide by array of switches SW2 (see Fig. 1), with the same condition as in the case of SW1, which means that only one switch can be in switch-on position and the rest have to be in switch-off position.

Finally, the output values of the decoder are inverted by logic gates (see Fig. 3).

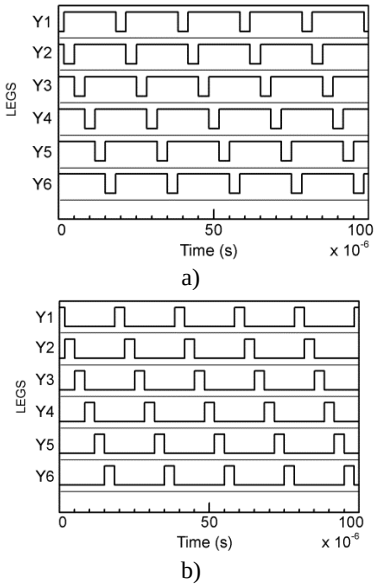

Fig. 3 a) Non inverted output from decoder, b) inverted output from decoder

B Legs of the PWM generator

The legs are designed in a way to be able to change their number and each leg of generator has to be identical to other one. Due to this fact, the following description will be done for only one leg.

Each leg of the generator is able to generate a PWM signal with a resolution of 400 discrete positions. Thus, the generator counter is counting to 400 every 20 µs (see Fig. 4).

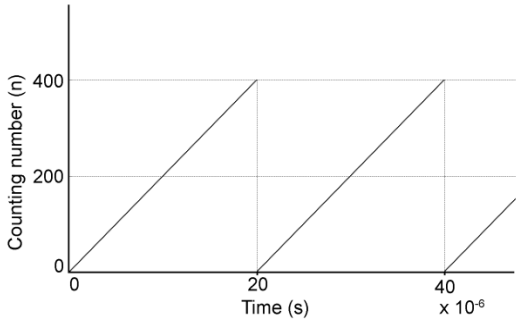

Fig. 4 Resolution of PWM

In order to achieve such resolution for output signal with 50 kHz frequency, it is necessary to connect the pulse signal with frequency of 20 MHz to the input of the counter. Three 4-bit counters are connected in series, because one 4-

bit counter cannot count to 400 (see Fig. 5). Therefore, the maximum counting value can be settled as 4095 and for counting to 400, it is sufficient to use only the first output bit from the third counter. The reset of all counters is realized by the synchronization pulse with frequency 50 kHz, which is generated by the divider. In this way, the counter resets and starts from the 0 after each sync pulse.

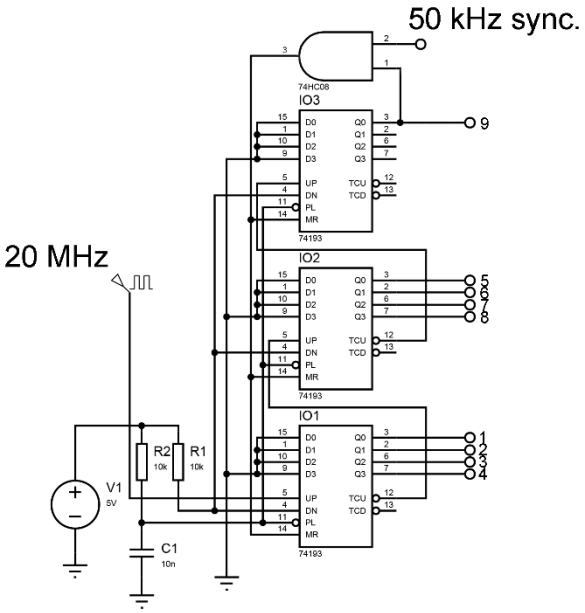

Fig. 5 Serial connection of the three 4-bit counters

The counter's output pins are interconnected with the inputs of three digital comparators connected in cascade and realized by IC 7485 (see Fig. 6). The 9-bit cascade comparator compares the desired value with the actual one in binary form. The actual value is obtained from the 9-bit counter outputs by the *A* bus. The desired value is adjusted by the *B* bus in the 9-bit digital form.

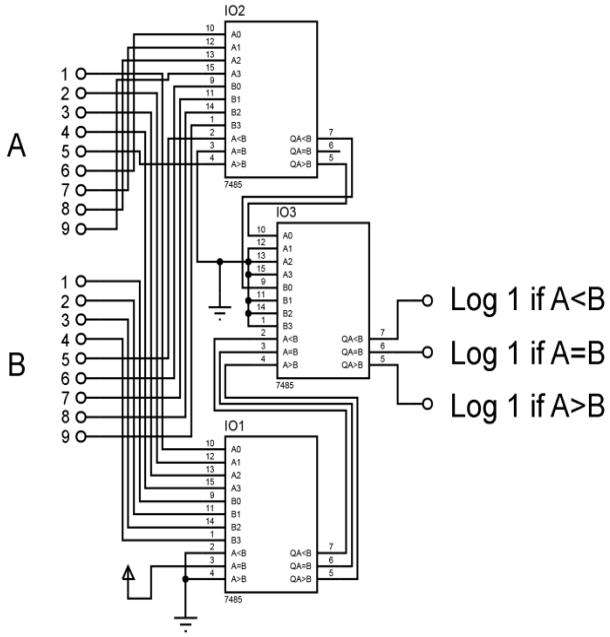

Fig. 6 Cascade connection of three digital comparators

The comparator provides three outputs. The first output has level log. 1, only at the moment, when the actual value is less, than desired. The second output is setting level log. 1, when the actual and desired values are equal. The third output sets log. 1, in the case when the actual value is greater than the desired one. For the desired PWM signal generation, it is possible to use the mentioned outputs.

The figure (see Fig. 7) illustrates the design of the one leg of the generator.

As was discussed, the pulse width control is possible to set by setting the digital inputs on *B* bus. It can be done for example by any microprocessor that has at least 9 I/O pins. In such way, the microprocessor doesn´t need to contain the PWM modulation ability.

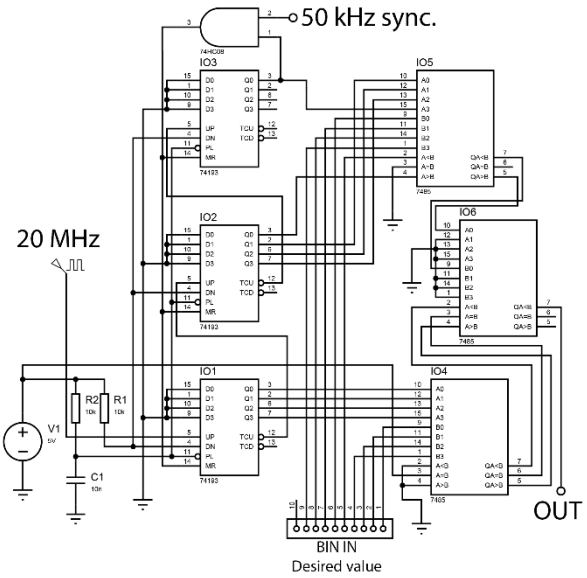

Fig. 7 One leg of the designed generator

3. SIMULATION RESULTS

The simulation model of the designed generator was created in Proteus 8 Professional simulation environment. This simulation program is able to simulate program including the microprocessor. The following simulations are performed with the help of ATmega328 microprocessor. The microprocessor had set values corresponding to the desired width of PWM in binary form, which are connected to the comparators. The comparators evaluate actual and desired values and generate output pulses.

The following two figures illustrate the simulation results obtained from a divider and legs of generator.

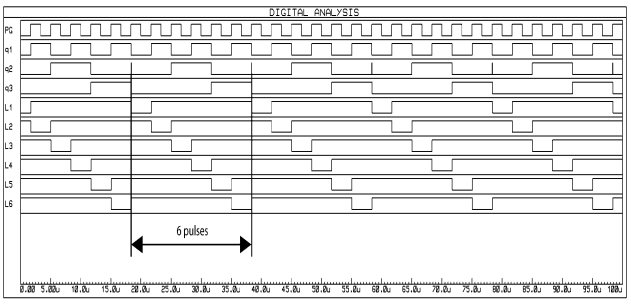

Fig. 8 Output signals from generator LTC1799 (PG), counter IC 74193 (q1-q3) and 10-bit decoder IC 7442 (L1-L6)

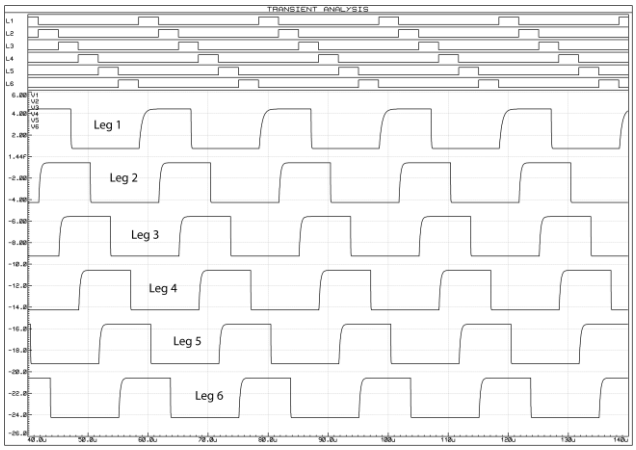

Fig. 9 Output inverted signals from decoder IC 7442 (L1-L6) and output signals from comparators IC 7485 (Leg1-Leg6)

4. EXPERIMENTAL RESULTS

The constructed prototype of generator was built and tested to verify the right principle of its operation.

The following oscillograms fully confirm the theoretical and simulation assumptions. The real microprocessor ATmega328 was used as a data entry circuit, similar as in the simulation.

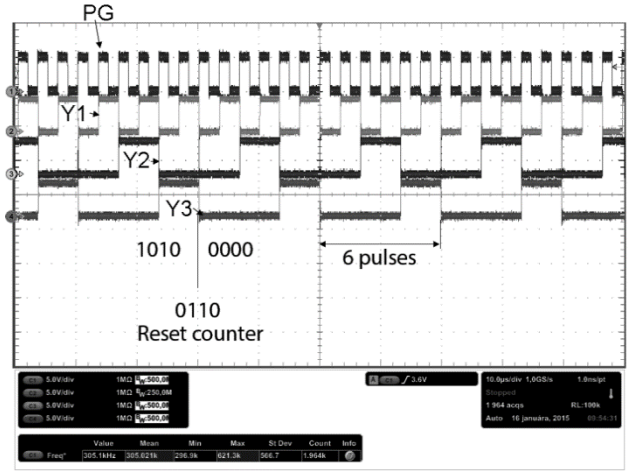

Fig. 10 Output signals from generator LTC1799 (PG) and counter IC 74193 (Y1-Y3)

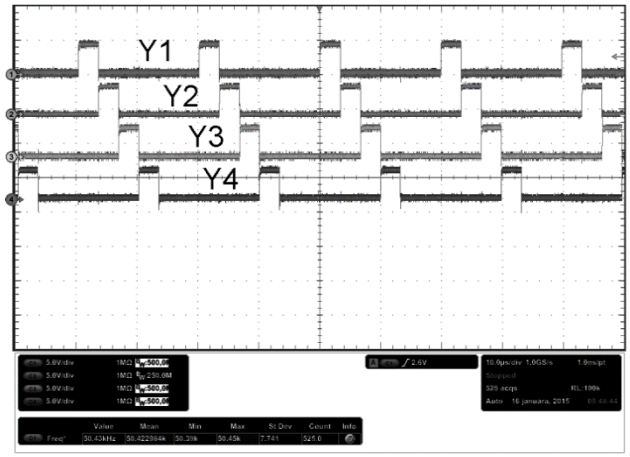

Fig. 11 Inverted output signals from the IC 7442 decoder

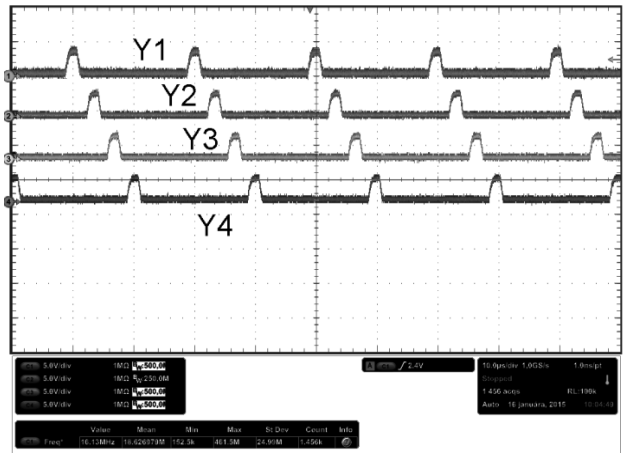

Fig. 12 PWM signals from comparator IC 7485

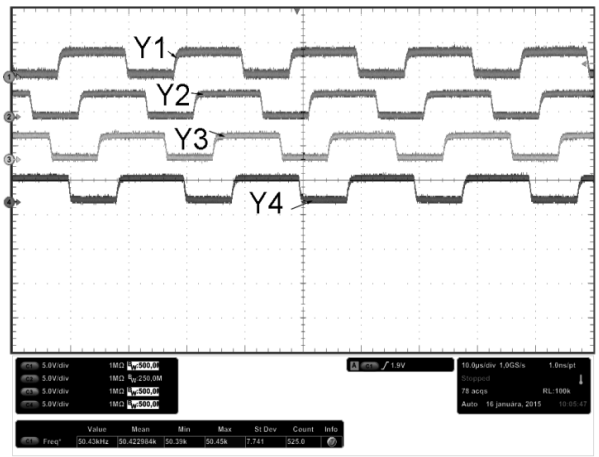

Fig. 13 PWM signals from the IC 7485 comparator

5. PROPOSED PRINTED CIRCUIT BOARD

PCB (**P**rinted **C**ircuit **B**oard) design was created in the Proteus 8 Pro environment (see Fig. 14).

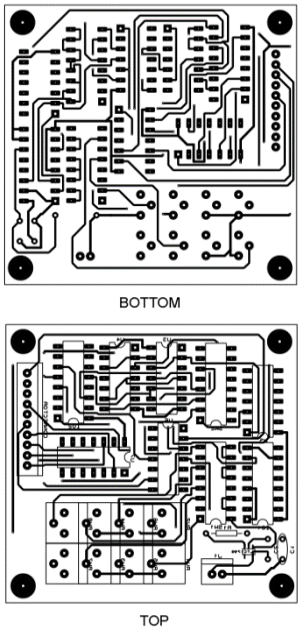

Fig. 14 Both sides of the designed PCB (divider)

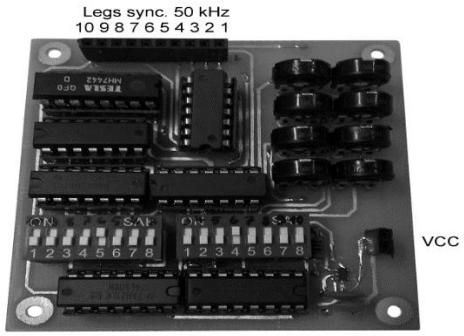

Fig. 15 Practical construction and design of the pulse divider

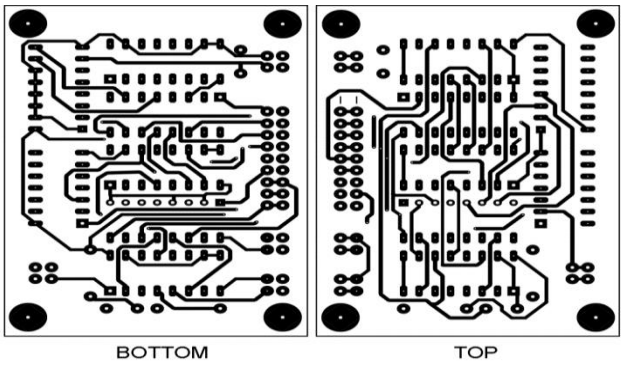

Fig. 16 Both sides of the PCB of the proposed PWM generator leg

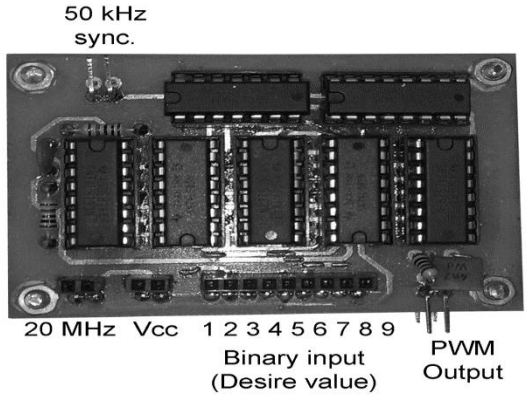

Fig. 17 Practical construction and design of the PWM generator, top view

Based upon the chosen concept of designed and realized generator, it is very easy to change the required number of legs, (see Fig. 18).

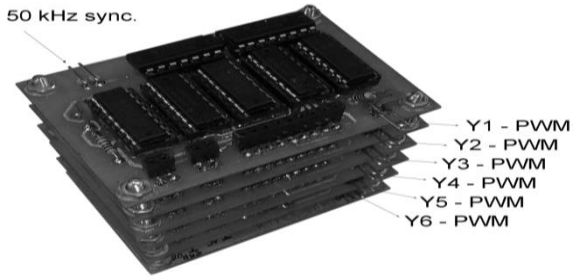

Fig. 18 Practical construction and design of the multi leg PWM generator

6. CONCLUSIONS

The results obtained by the simulation and from realized measurements are confirming the operational correctness of designed and realized generator, which can be used for control of multi-phase buck-boost converters. The structure is designed in such a way, to be able to easily change the number of legs, number of discrete states of width at PWM and also the output frequency, which can reach up to hundreds of kHz. Control of this concept is provided easily by the 8-bit microprocessors. It means that the design doesn´t require expensive or very fast microprocessor. Because of this it is possible to realize the generator, which is inherently cheap and sufficiently precise.

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BIOGRAPHIES

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Dobroslav Kováč - He finished his studies in 1985 at the Technical University of Košice, Department of Electrical Drives, area - Power electronics with excellent evaluation. Then he worked as a research worker at the Department of Electrical Drives. His research work was focused on the practical application of new power semiconductor devices. In 1989 he got the Award of the Minister of Education for the Development of Science and Technology. From 1991 he has worked as assistant lecturer at the Department of Theoretical Electrical Engineering and Electrical Measurement. He got his doctoral diploma in 1992 for the work on the field of power electronics. From 2000 he has worked as professor and his working interest is now focused mainly on the field of computer simulation of power electronic circuits and automated computer measuring.