FUNCTIONAL SWITCHING MATRIX FOR AUTOMATIC ANALOG CIRCUIT SYNTHESIS

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ABSTRACT

Synthesis of analogue circuits, most commonly achieved by heuristic methods. In this paper we show that the circuit topology used in the development of what semi-automatic and automatic options available. In this article we'll show also how the many alternatives we can reduce the number of attempts, to make the process more efficient. Method described in this article illustrates the applicability of the solution using a simple example. This approach may be important later in the digitally configurable programmable analog circuits (FPAA) analog synthesis system perspective. The switch matrix as described by using the chances of these circuits may be extended.

Keywords: analog circuit, semi automatic synthesis, heuristically feedback

1. INTRODUCTION

An analog electronic circuit function (Γ_c) and behaviour (*f*) is determined by the parameters of the used components ($\overline{P}$) and the connect topology (*n*), formal according to equation (1);

$$\Gamma_c = f(n, \overline{P}). \tag{1}$$

The circuit function is of course not an exact definition, but it can mean for example from input to output time domain determined amplitude function, frequency-domain amplitude characteristic and so on. The used circuit description depends on the suspected or the realized function of circuit [1][14][17].

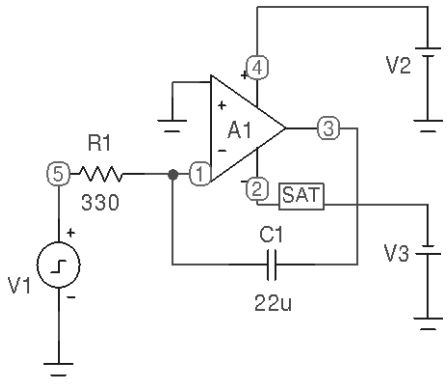

Fig. 1 Integrator circuit

Parameter (*n*) describes the network of the discrete component; in there pins are well determined connected to each other.

In equation (1) the $\overline{P}$ parameter is a scalar vector, that contains the relevant parameters of used electronic parts in formal equation (2);

$$\overline{P} \in p_0, p_1, p_2 \ldots p_n, \tag{2}$$

where: p_n the significant parameter of electronic part, for example resistance of a resistor, capacitance of the a capacitor, h_{21} of a bipolar junction transistor…etc. [15][16].

On Fig. 1 is seen, as above example an integrator circuit. This circuit contains an operational amplifier (A_1), a square wave input generator; (V_1, or X1) U_{pp}=2V, U_{offset}= –1V, two power source; (V_2, V_3 or X2) with ±15V, a feedback capacitor (C_1) its value is 22μF, and a resistor (R_1) it's value is 330Ω. These parts lists and entering a value is defining of the $\overline{P}$ vector [18].

Table 1 The Integrator circuit connection network

Net	Part	Pad	Pin
GND	IC1	1	+IN
	X1	1	S
	X2	2	S
N$1	C1	1	1
	IC1	3	–IN
	R1	2	2
N$5	R1	1	1
	X1	2	S
N$3	C1	2	2
	IC1	4	OUT
	X2	1	S
VCC–	IC1	2	V–
VCC+	IC1	5	V+

Tab. 1 shows a connection network in short form a *netlist* circuit's of Fig. 1. This net list describes the nods of circuits (N$1, N$3, N$5). The nods N$3 connect two parts, a capacitor (C_1), and the output of amplifier (A_1) with four pads of integrated circuit, and output of circuit to X_2 connector [2]. (X_1 and X_2 input and output points which used in the simulation in timedomain.)

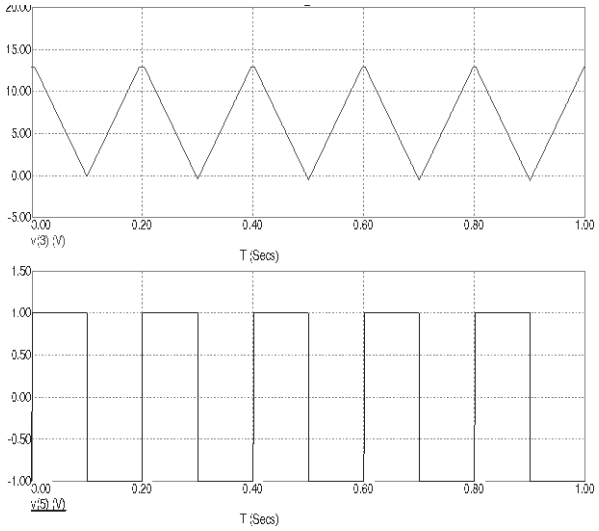

Fig. 2 Time domain simulation of integrator circuit. Bottom input signal, above the output

Nowadays the development of such a circuit heuristic means. We know the circuit operation, the availability of parts and components to form a network with the appropriate values [3][4]. To draw the circuit CAD tools are used, as well as circuit simulation. Network of Tab. 1 is generated from wiring diagrams [5][14][15] [16] [17] [18].

Computing environment is possible to check by circuit simulation software the operation of the realized circuit. Fig. 2 shows in time domain the circuit operation from input to output [6].

So the traditional analog circuit developing methods we summarize in flowchart of Fig. 3. As shown the CAD development tools are used, but is fundamental to the existing electronic engineering knowledge, experience, the heuristic is dominant. From the result of created circuit's simulation we must often feedback to every level of developing and to the art of simulation as well and comparison with the author's results should be given [7][8] [16] [17] [18].

2. ANALOG CIRCUIT REALIZATION BY A SWITCHING MATRIX

Theoretically, if we have *n* numerous electronic components each of them has got φ_i pins which are necessary to properly connect with a wished analog circuit. If every possible way we want to create a circuit network, we need a matrix that consists of *o* number of columns according the (3);

$$o = \sum_{i=0}^{n-1} \sum_{j=0}^{\phi_i - 1} c_{ij}, \tag{3}$$

where for $A_{m(i,j)}$ is true according (4);

$$A_{m,(i,j)} \in [0,1]. \tag{4}$$

On Fig. 4 theoretical arrangement of a switching matrix is shown. This matrix consists of electronic part's dev_0–dev_n leg wires as columns c_{00}–$c_{n(\varphi-1)}$, and row wires for possible interconnections r_0–r_{m-1}.

In (4) *0* means no connection between column and row wires, and *1* case is have got, this is actually a switch function, which is described of turned *ON* and *OFF* state. On Fig. 4 we signed this function by a switch k_g [7][8].

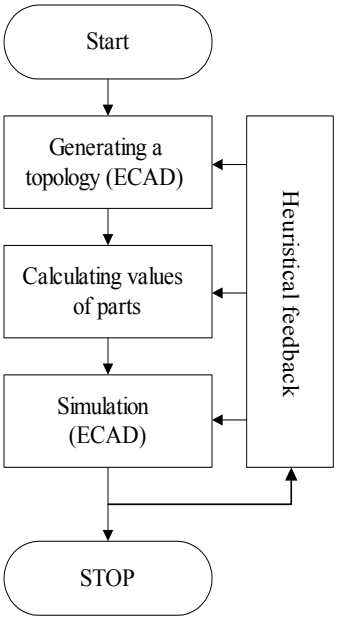

Fig. 3 Flowchart of an analog circuit developing with using of CAD abilities

It can be seen that the pins of electronic components and the interconnection wires formed from a matrix of **m**x**n** type, where **m**=**n**, so there is square matrix, which contains all the possible options of connections, according in equation (5):

This square matrix from equation (3) contains numerous cross points according to (6) is;

$$A_{m,(i,j)} = \begin{bmatrix} b_{0,(0,0)} & b_{0,(0,1)} & b_{0,(1,0)} & b_{0,(1,1)} & b_{0,(1,2)} & b_{0,(2,0)} & b_{0,(2,1)} \cdots & b_{0,(n,\phi-1)} \\ b_{1,(0,0)} & b_{1,(0,1)} & b_{1,(1,0)} & b_{1,(1,1)} & b_{1,(1,2)} & b_{1,(2,0)} & b_{1,(2,1)} \cdots & b_{1,(n,\phi-1)} \\ b_{2,(0,0)} & b_{2,(0,1)} & b_{2,(1,0)} & b_{2,(1,1)} & b_{2,(1,2)} & b_{2,(2,0)} & b_{2,(2,1)} \cdots & b_{2,(n,\phi-1)} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ b_{m-1,(0,0)} & b_{m-1,(0,1)} & b_{m-1,(1,0)} & b_{m-1,(1,1)} & b_{m-1,(1,2)} & b_{m-1,(2,0)} & b_{m-1,(2,1)} \cdots & b_{m-1,(n-1,\phi-1)} \end{bmatrix}. \tag{5}$$

$$C_p = o^2 . \quad (6)$$

Thus, the number of theoretically possible different topology (T_n) from equations (5) and (6) is;

$$T_n = 2^{C_p} . \quad (7)$$

Fig. 4 layout and description of equations (5) and (6) are so perfectionist that includes abilities of all the parts legs wires the possibility of connecting a node, as well as the possibility of all parts foot stand-alone, a unique node [9][10].

3. OPTIMIZATION OF A SWITCHING MATRIX

In the previous paragraph the possibility formation of the theoretical switching matrix is shown. According to the described solution we generate from the circuit of Fig. 1 or net list of Tab. 1 in matrixes in Fig. 5.

In the theoretical matrix (Fig. 5, 6) the number of connection, according equations (6) and (7) was: $r_{m-1} \cdot c_{n(\varphi-1)}$, actually in examples are $C_p=17^2$, $C_p=289$ so the abilities topology are $T_n=2^{289}$, $T_n=9{,}94 \cdot 10^{86}$.

These values at the proposed structural switch matrix are in order to form; $C_p=17 \cdot 10$, C_p =170, and $T_n=2^{170}$, $T_n=1{,}49 \cdot 10^{51}$. The different according T_n parameter in $\sim 10^{35}$.

Other mitigation options appropriate management of common GND node, and self-evident is providing of active device's power supply [11][12]

A special heuristic approach is the elimination of not used rows of matrix, on Fig 6 from r_8-r_{16}. So the number of T_c is "only" $1{,}2 \cdot 10^{24}$.

4. AUTOMATIC SYNTHESIS BY SIMULATION FEEDBACK

In the paragraph 3 we showed how we are able to reduce the number of abilities analog circuit topology. We have shown that by choosing of appropriate structural switching matrix the number radical reduced. It is very important because we propose such a method that is automatically should generate different schemes of analog circuit.

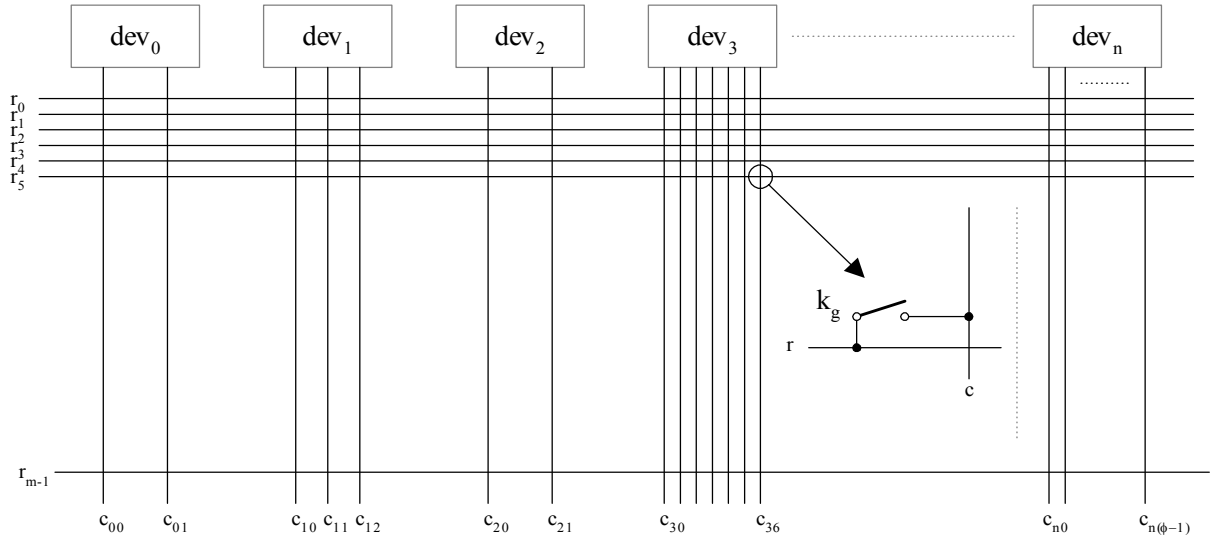

Fig. 4 Theoretical arrangement of a switching matrix for the evolving every abilities connections

On Fig. 5 it can followed that every nods of net list means a row of matrix; r_0=GND, r_1=N$1, r_2=N$2, r_0=N$3, r_0=N$4, r_0=N$5. You can see that the rest of any unused nods abilities from r_6–r_{16}.

The electro technical or physical reason of the not used abilities is understandable, because it is meaningless to connect, for example, two power supplies (N_2, N_4), or output of operational amplifier (N_3) with input signal source (N_5). Of course one can find too much refusal of this kind.

So our proposal is such **structural switch matrixes** which can not afford such unusual theoretical, often catastrophic result inflict solution.

On the other hand, it is necessary to minimize number of cross points, because the number of ability network according to the equation (7) easy to be huge combination.

On Fig. 6 you can follow the whole proposed methods [11][12][13].

In a "Generating of topology" block a C language program is generated by a combinatory method. We give in "Setting of relevant parameter" block one-one suitable parameter for the used electronic parts.

Then by means of a simulation program we check the behaviour of the created circuit for example in time domain we check. If the characteristic of simulated circuit does not fit, we generate a new one.

If the behaviour of circuit is suitable we need only to set the optimally values of parameters.

5. CONCLUSIONS

It is alleged that a well-designed matrix prevents the development of adverse topologies, and significantly reduces the number of possible conceptual networks.

The above process is relevant at application of Field Programmable Analog Array (FPAA) circuits and special programmable analog peripheries of PSoC technologies.

This article provides a solution the applicability of high performance computers and advanced cross-bar switch circuits appearance.

The proposed methods are extendable for the system generated from functional blocks, and subsystems.

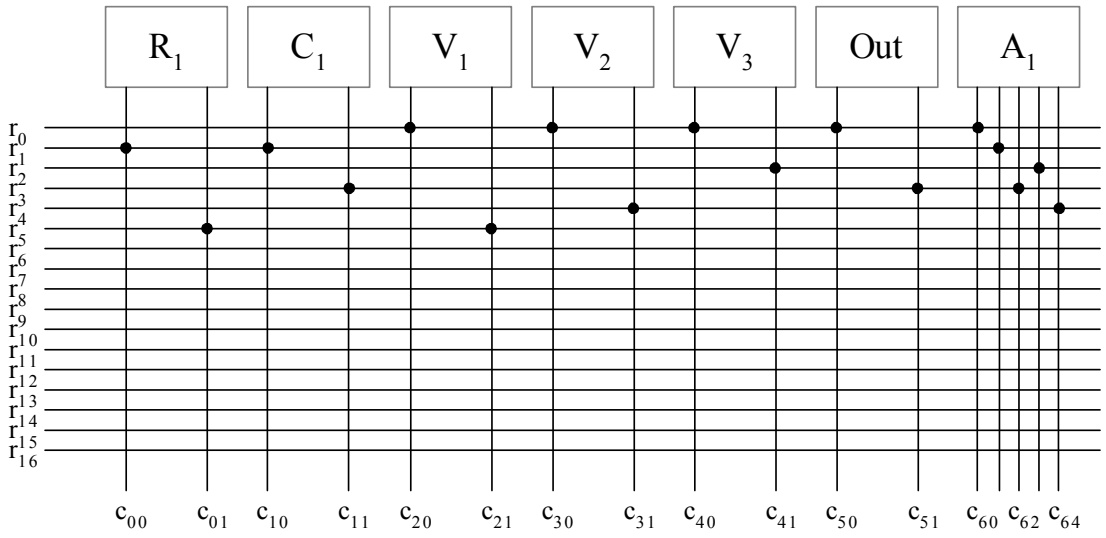

Fig. 5 Integrator circuit realization in actually connections on a switching matrix

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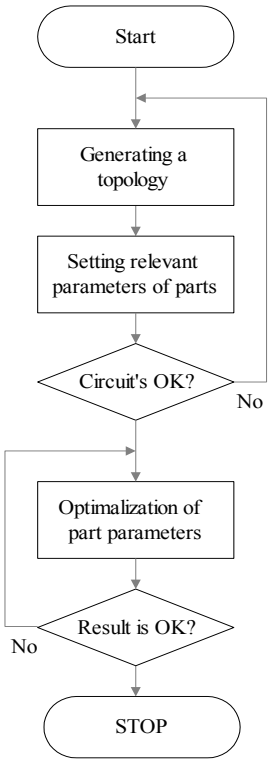

Fig. 6 Automatically generation of analog circuit with two level feedbacks

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BIOGRAPHIES

György Györök was born on 3. September 1958. In 1980 he graduated (BSc) at the Department of Computers Technology Institute in Kandó Kálmán College and 1988 (MsC) of the Faculty of Electrical Engineering at Technical University Budapest. He defended his dr. univ. in a special questions of computer peripheries 1994, and PhD in the field of programming analog circuit in 2009; his thesis title was “Synthesis of Systems build Programmable Ana-log Circuits “. Since 1989 he is working as a tutor with the Department of Computers Technology, and later Alba Regia Technical Faculty of Óbuda University. His scientific research is focusing on robust electronic circuit realization, reconfiguration of analog and hybrid circuit, and cooperation of embedded microcontroller and application of programmable electronic circuit.