DYNAMIC DAC TESTING BY REGISTRATION OF THE INPUT CODE WORDIN EQUALITY WHEN THE DAC OUTPUT MATCHES A REFERENCE SIGNAL

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ABSTRACT

The characterization of high resolution Digital to Analog Converter (DAC) involves new problems caused by their high performance. This paper presents a new method for measuring the characteristics of high resolution DACs under dynamic condition. The main principle of the proposed method is the conversion of the DAC analog output voltage to a digital code. The one that is corresponding to the equality of the DAC output voltage and reference signal by using a fast comparator, a dithering DAC and an accurate dc voltmeter. The output of the comparator is used as the control signal to register the digital input code word of the DAC in a fast memory. After digital processing the registered record of digital code words is used to determine the Integral-nonlinearity (INL) and Differential-nonlinearity (DNL) of the DAC under test.

Keywords: *Digital to Analog Converter (DAC), dithering, DNL, INL,comparator*

1. INTRODUCTION

The exponential growth of electronic systems including digital signal processing led to an increasing interest in data converters. In many ones the digital information must be converted to the analog domain through a Digital-to-Analog Converter (DAC). However, today electronic devices integrates more and more features, and each requires a higher requirements for further increase the amount of processed data, speed as well as accuracy and quality. Such a significant increase of performance and accuracy of today's electronic devices also requires the use of highly accurate/precise, rapid and linear DAC converters. The use of such DACs requires a simple and reliable testing procedure available to do in the commonly equipped laboratories.

Many DAC procedures have been proposed by different authors [1] - [13]. Some of them have been assessed by both simulation and experimental implementation. The authors proposed in a page mentioned above [13] a dynamic DAC testing procedure based on the conversion of the DAC output level into a time interval. One of the advantages to compare with the previous project and standardized methods was the transfer of precision requirements from the waveform recorders to the time interval measurement, which can be measured with higher accuracy than the dynamic output voltage. The drawback of this method was that besides the comparator accuracy the time jitter of the clock frequency corrupted the final accuracy.

The principle of the proposed method is to compare the dynamic output voltage of the DAC under test with the reference dc voltage by using a comparator. In the moment when DAC analog output voltage exceeds the reference level, the registration of the corresponding digital input code is in use. The output of the comparator is used as the control signal to register the digital input code word of the DAC under test in a fast memory. This approach allows assigning to the DAC input digital code the precise (real) value of the DAC output voltage which is utilized as the reference voltage.

There are two main benefits of the proposed methods. Insensitivity to frequency jitter,while it doesn`t requires the use of an ultra fast converter, The other one is the possibility to suppress comparator`s error by numerical correction count on facts that delay remains constant.

2. THE PROPOSED METHOD FOR DAC TESTING

The analog output voltage of the DAC under test (DAC UT) corresponds to the conversion of an input digital sawtooth sequence to the analog domain (Fig.1). Once the DAC analog output voltage exceeds the reference level the digital input code is stored to the fast memory. This approach allows assignation the DAC input digital code to definite real value of the DAC output voltage which is utilized as the reference voltage. In order to avoid quantization uncertainty the triangular dithering voltage with known peak-peak value is superimposed to the reference voltage ($U_{SUM} = U_{DC}+U_{DITH}$). The required amplitude of dithering is achieved by using an appropriate resistive divider. The impact of real dithering amplitude is being suppressed by digital post processing. The distortion of triangular dithering voltage can involve uncertainty. The amplitude reduction by the passive divider decreases the existing distortion of the generated dithering voltage at the output of the dithering DAC.In addition the amplitude reduction allows the use the dithering DAC with a lower resolution than the resolution of the DAC under test.

The quantization error is avoided by the digital averaging of registered codes during testing interval which corresponds to the integer number of dithering signal periods. The output value from the precise dc voltmeter during one testing interval determines reference voltage with required accuracy. The impact of dithering voltage is suppressed because of averaging effect during integer number of dithering periods. The metrological traceability of the proposed method is being protected by the precision of utilized voltmeter.

The error offset and comparator time delay are reduced by the digital post processing. INL error of DAC UT full scale range should be according to the terminal definition

equal zero at the beginning as well as in the end.The difference achieved between measured level and theoretical one is used to correct the whole output DAC range. The only consideration is that time delay is constant or is changing linearly along full scale range. The main problem related with comparator is oscillation around the comparation level. The small hysteresis suppressed partially this problem. Another possibility is the implementation of nonlinear digital filtering of registered data.

A block diagram of the measurement system is shown in Fig. 1.

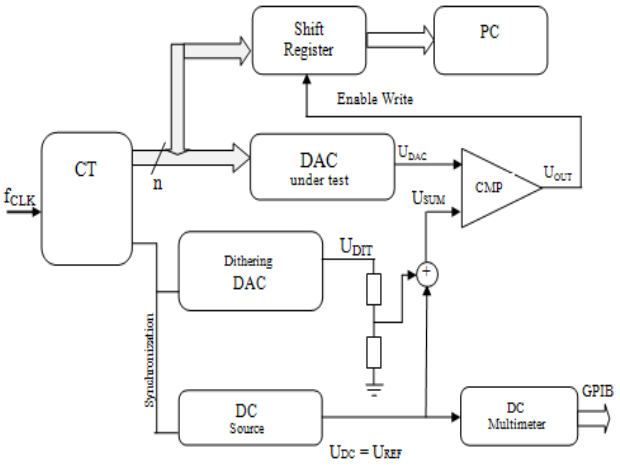

Fig. 1 Block diagram of the proposed measurement system

One measuring cycle contains L periods of the sawtooth voltage generated by the DAC under test and M periods of the dithering voltage, as shown in Fig. 2. The peak to peak value of the dithering voltage W corresponds to a few LSBs of the DAC under test. The DC voltage is measured by the precise dc voltmeter during the measuring cycle.It average and obtain only precise value of the voltage from dc.

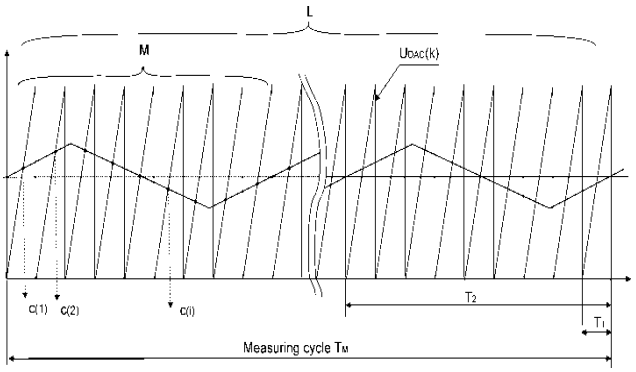

Fig. 2 Analog output voltage $U_{DAC}(k)$, from the DAC under test and reference voltage U_{REF} as superposition of the dithering voltage U_{DITH} on DC voltage Ua

Therefore, the measurement cycle is defined as $T_M = L.T_1 = MT_2$ where T1 is the period of digital sawtooth at the input of the DAC UT and T_2 is the period of the dithering voltage. The sawtooth voltage at the input of the DAC under tests in the period with is generated linearly from 0 to 2^N-1 levels. The period T_1 of the analog voltage generated by the DAC under test is given by:

$$T_1 = \frac{2^N}{f_{CLK}} \tag{1}$$

wheref_{CLK} is clock frequency for setting a new digital input code word. The period of generated analogsawtooth voltage T_1 can be adjusted by changing clock frequency f_{CLK} and in such a way the slope of the tested signal can be changed.

In order to avoid coherence between dithering voltage U_{DITH} and sawtooth voltage the constant L and M must be ordinary prime numbers. To meet the described requirement, we can write the following statement for periods of both signals and also the constant L and M:

$$\frac{T_2}{T_1} = \frac{L}{M} = \frac{f_1}{f_2} \tag{2}$$

During each sawtooth period in the raising phase the comparator determines the instant when the output voltage of the DAC under test exceeds for the first time the voltage U_{SUM}(Fig. 3), which is the sum of the dc voltage (U_{DC}) and the dithering voltage (U_{DITH}). This time instant is determined by a positive derivation of the output voltage of the comparator U_{OUT}. We can write the following condition for this instant:

$$U_{DAC}\left(k(i)\right) \geq U_{SUM} = U_{DC} + U_{DITH} \tag{3}$$

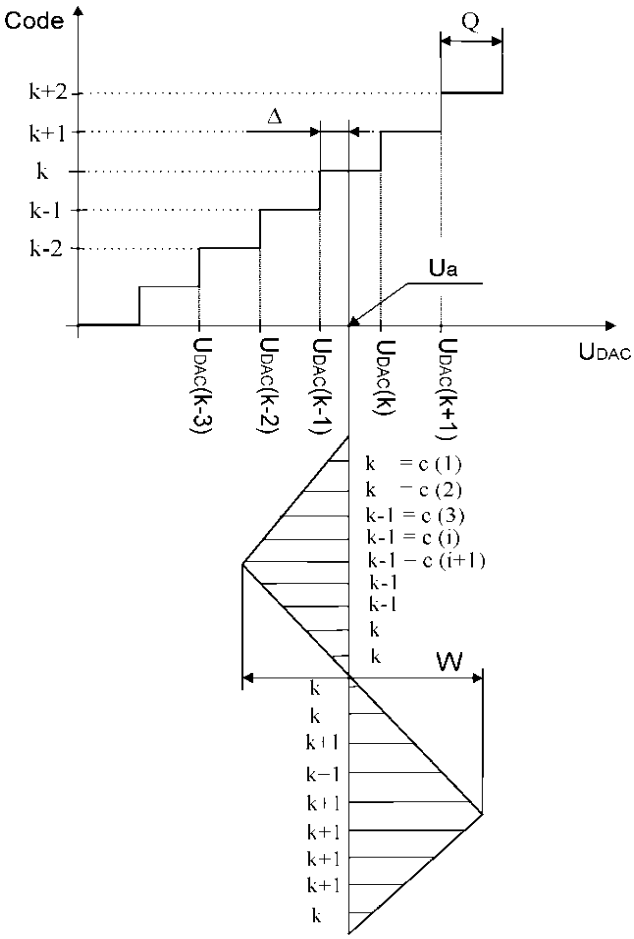

Fig. 3 View of transfer characteristic tested DAC together with reference voltage U_{DC} and dithering voltage U_{DITH} and also the way of obtaining array of input digital code words

The recorded code word c(i) from the DAC under test input match the following conditions:

$$\begin{aligned} &U\left(k\left(i,j\right)\right) \geq U_{SUM} = U_{DC} + U_{DITH} \\ &U\left(k\left(i,j-1\right)\right) < U_{SUM} \\ &c\left(i\right) = k\left(i,j\right) \end{aligned} \tag{4}$$

During one measuring period T_M the shift register stores an array of L values c(i), i = 1....L. Those values code words c(i) are directly influenced by the difference between U_{DAC} (k) and voltage U_{DC}. In real conditions the adjusted reference voltage U_{DC} should be set as close as possible to the measured code level U_{DAC}(k). The measured deviationΔbetween real value U_{DAC} (k) and the reference voltage U_{DC} measured by a precise voltmeter is being determined by the following procedure.

At the end of measurement cycle specified by time interval TM the registered array of c(i) values is transferred to a PC. Here the c(i) array is being transformed into a new array p(i), i = 1....L, where for each i value p(i) suit the following condition:

$$\begin{aligned} &c(i) \leq k \quad \Rightarrow p(i) = 0 \\ &c(i) > k \quad \Rightarrow p(i) = 1 \end{aligned} \tag{5}$$

This transformation serves mainly to suppress the influence of neighbouring quantization levels errors and nonlinearities dithering voltage on the overall accuracy of measurement. In addition makes the measurement almost completely independent of the amplitude and period of used dithering, which considerably simplifies the measuring conditions. From this obtained array p(i) is then calculated the average value:

$$\overline{P} = \frac{1}{L}\sum_{i=1}^{L} p(i) \tag{6}$$

The deviation Δ between real value U_{DAC} (k) and analog voltage U_{DC} is than determined by:

$$\Delta = W\left(\overline{P} - \frac{1}{2}\right) \tag{7}$$

The exact value of the analog output voltage of the DAC under test for code k is determined by:

$$U_{DAC}(k) = Ua - \Delta = Ua - W\left(\overline{P} - \frac{1}{2}\right) \tag{8}$$

If the real value of the DAC analog output voltage is known then we can determine the value of the integral nonlinearity from:

$$INL(k) = \frac{U_{DAC}(k) - k * Q}{Q} \tag{9}$$

The INL has to be corrected in both ends of FS to zero values. To increase the precision of the determination of the resulting values and the suppression of random effects and interference entering the measurement stand dithering with amplitude several times greater than the amplitude of the ideal quantization step.

3. RESULTS

The proposed approach has been evaluated both by simulation (modelling a DAC with imposed nonlinearities) and experimental. Figure 4 shows front panel of simulator of a DAC testing by using the proposed method, created in LabView environment. The simulation of measured 8-bits DAC is done by proposed method only under following circumstances:number of sawtooth period L=10.000, number of dithering periods M=957 (this ensure that the ratio between frequencies of the DAC analog output voltage and dithering signal is not an integer) The amplitude of the used dithering voltage is equal to 10 LSBs of the DAC under test. In addition, there was added Gaussiannoise with a standard deviation of 0.25LSBto the simulation.

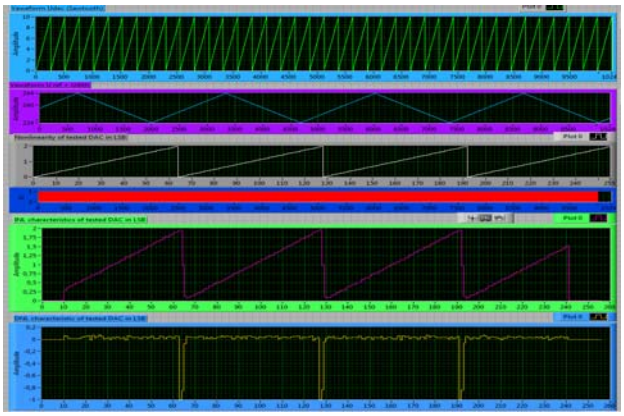

Fig. 4 Front panel of simulation of DAC testing by registration of input code in the moment when the analog output from DAC under test exceeds the reference one for 8-bit DAC

Simulation confirmed the expected ability of the method to measure INL and DNL characteristics with high resolution (below 0,1LSB) and also the independence the amplitude and period of used dithering signal. The problem with precise measurements (including the proposed method) is the noise and interference, which affect the resulting measurement accuracy. By using the average, the adverse affect is suppressed down.

The experimental validation of the proposed method was performed by using 8-bit DAC, commonly available comparator LM 319N and the reference signal (U_{SUM}=U_{DC}+U_{DITH}) was generated by a DAQ card PCIe 6251. As expected, the biggest experimental problem to solve was the influence of noise, which caused oscillation of the comparator at the moment of comparison. The oscillation of comparator was suppressed by using hysteresis (HYST=1,6mV corresponding to approximately 1/23LSB of tested DAC). There were another difficulties discovered during the experimental preliminary validation: systematic error and glitch on DAC analog output, which can cause incorrect assessment. The mentioned difficulties mightresult into load of incorrect code words. Negative effects of noise on the measurement discovered during experimental verification were

suppressed by using a more suitable arrangement grounding and rearranging the entire involvement. Registering incorrect code words was suppressed using an algorithm that can remove most of the incorrect code words in the registered sequence. A dynamic INL and DNL characteristic of the DAC under test obtained by the proposal method under following condition: f_{CLK}= 512kHz, triangular dithering with 10LSB peak to peak amplitude, value L=10.000 and M=871 are shown in Figure 5. The static INL and DNL characteristic obtained by a traditional method is shown in Fig. 6.

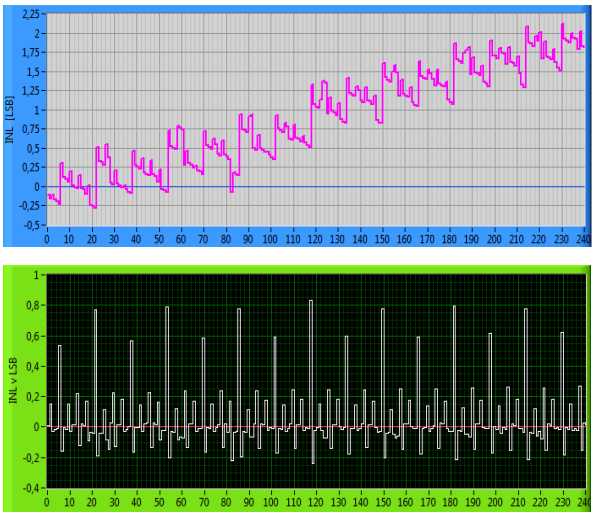

Fig. 5 INL and DNL characteristic of8-bit DAC obtained by the proposal method under mentioned condition

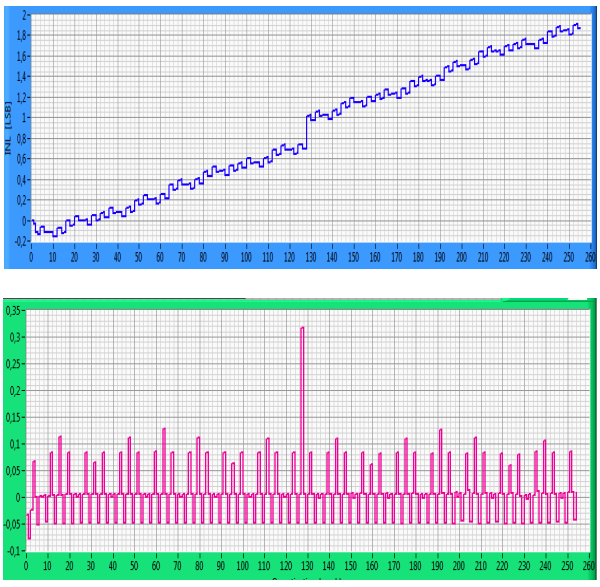

Fig. 6 Static INL and DNL characteristic of tested 8-bit DAC obtained by known procedures using the precise digital voltmeter Agilent HP34410A

4. CONCLUSIONS

In the article is DAC performance assessment presented by new method for design and implementation of the measurement. The advantage of the proposed method is based on the determination of the functional DAC parameters (INL and DNL).It is done in dynamic mode using predominantly digital signal processing of registered data. Another advantage of the proposed method is the possibility to test DAC properties for discrete values of slope S. The only restriction for slope selection is that L/M must be ratio of two prime instruments or the time step must be integer number of minimal time intervals.

The method relies on the features of the precise dc voltmeter. DC voltmeter is the instrument which requires accuracy of highest to compare with the other instrument for the same price. A fast and accurate comparator is required. The impact of time-invariant errors could be removed by digital post processing.

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